Department of Electrical Engineering
Visvesvaraya National Institute of Technology

Declaration

I, JAGANNATH BANIK, certify that I worked on the "Pulse width modulation strategies for common mode voltage elimination in multilevel inverter fed induction motor drive" project at the Visvesvaraya National Institute of Technology in Nagpur's Department of Electrical Engineering. This work has never been submitted before, in whole or in part, for the purpose of earning a degree or diploma from this university or any other. It is completely original.

JAGANNATH BANIK
Date: May 30 2025.

Certificate

This is to certify that the project titled "Pulse width Modulation strategies for common mode voltage elimination in multilevel inverter fed induction motor drive", submitted by Jagannath Banik in partial fulfilment of the requirements for the award of the degree of Master of Technology in Power Electronics and Drives, VNIT Nagpur. The work is comprehensive, complete and fit for final evaluation.

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PULSE WIDTH MODULATION STRATEGIES FOR COMMON MODE VOLTAGE ELIMINATION IN MULTILEVEL INVERTER FED INDUCTION MOTOR DRIVE

Dissertation submitted to
Visvesvaraya National Institute of Technology, Nagpur in partial fulfilment of requirements for the award of degree of

Master of Technology
in
Power Electronics and Drives

By

JAGANNATH PRANKRISHNA BANIK
(MT23PED005)

under the Guidance of

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JAGANNATH BANIK

ABSTRACT

Nowadays, Pulse width modulation strategies have become widely effective due to their application in variable frequency drives in industries. These variable frequency drives use power electronic devices to control motor speed and torque performance. As a result, a lot of manufacturing industries have been using these VFDs. The inverters present in this control the amplitude and frequency of AC supply using multiple PWM techniques. Inverters are generally used to convert DC power to AC power of some specified magnitude and frequency of the output voltage. However, in the process of providing dynamic performance like required output voltages, PWM inverters have introduced some serious problems like induction of shaft voltage, bearing currents, motor insulation breakdown and electromagnetic interference (EMI) issues. As a result, the lifespan of the motor reduces which endangers the whole drive system. These all problems have been caused by the pro-duction of common mode voltage CMV. It produces serious Electromagnetic interference (EMI) in modern PWM-operated electric drives. These problems will be increasing more as our industries move to the wide-bandgap (WBG) semiconductor devices that operate at high switching frequencies. A lot of industries relying on large motors use the common mode voltage reduction methods to protect the machines from malfunctioning. In induction motor drives, the common mode voltage is produced between the star point of the motor and the ground of the system.

Further multi-level and multi-phase systems provide a greater degree of freedom to reduce common mode voltage. The type of inverter decides the number of output levels and phases. Multi-level inverters generally produce the number of levels in output voltage per phase as greater than or equal to three. This allows the VSI to operate on greater voltages. Multi-level inverters also provide a better waveform quality of output voltage by reducing the total harmonic distortion THD, which will generally be less than two-level inverters. It also produces reduced EMI. Various topologies are available in multi-level inverters, out of which neutral point clamped inverter (NPC), Flying capacitor (FC), the cascaded H bridge(CHB)and T type configuration are well-known.

Similarly, multi-phase inverters are having greater flexibility in reducing common mode voltage over conventional three-phase inverters. They have a lot of benefits like higher power density, improved efficiency, power splitting among the phases, lower EMI, fault-tolerant capability, improved reliability, etc. Even though the complexity is increased, these are mostly used when uninterrupted operation is required in applications like ship propulsion, EV drives, etc.

The proposed work includes the reduction of common mode voltage in conventional three-phase two-level inverters by using various discontinuous bus-clamped PWM techniques on an inverter-fed induction motor. Further, to analyze the degrees of freedom to control CMV, a three-phase three-level NPC converter has been used. Control techniques like a double modulating wave along with its reversal and carrier-based PWM techniques based on a generalized algorithm are applied to remove the instantaneous CMV. An attempt to observe the reduction of CMV values in a multi-phase drive specifically on a five-phase three-level converter is also simulated. Techniques like phase disposition (PD) and phase opposite disposition(POD) have been applied and CMV is reduced. In all these methods performance parameters like torque ripple, speed response, THD and current ripples have been evaluated and compared using a software tool MATLAB SIMULINK.

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Nomenclatures

The following list describes the symbols used in this document:

λ	Flux linkages
ω	stator magnetic speed in radians per second
ω_r	Rotor speed in radians per second
B	Frictional coefficient
i_{NP}	Neutral point current
J	Moment of inertia
L_m	Mutual inductance
L_r	Rotor inductance
L_s	Phase inductance
R_s	Stator resistance
T_e	Electro magnetic torque
T_l	load torque
V	Supply Voltage
V_{AO}	Pole voltage of A phase

List of Publications

Jagannath Banik, B. S. Umre. "A CB-PWM Technique for Five-Phase Three-Level Voltage Source Inverter." In 10th International Conference on Advanced Materials Development & Performance (AMDP), Tokushima University, Japan

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Chapter 1

INTRODUCTION

1.1 Background

Any industry needs to install different kinds of electric motors as the prime mover for the driving equipment in its manufacturing processes. Electric drives are mainly employed for systems that require motion control – like transportation systems, fans, robots, pumps, machine tools, etc. They have several inherent advantages such as flexible control characteristics, self-starting, a wide range of speed, torque profile, greater power, high efficiency, good power factor, lower noise and less maintenance. They are simple, rugged, self-starting, and low-cost rotor structures that require less maintenance. Nevertheless, there are certain limitations such as maximum power per phase, current limited by the conductor size in a given frame, higher amplitude, low frequency of torque ripple, higher operating noise, mechanical vibrations and high-power converter devices. To overcome these constraints, the development of alternate motors associated with power converter topologies and controllers for medium and high-power energy conversion systems is required. These features have inspired more to show interest in (5-ϕ) inverter-fed induction motor drives [1].

Voltage source inverters are power electronic6 converters that convert fixed DC voltage to AC voltage. These are the most extensively utilized converters with power ratings ranging from fractions of KW to MW with controlled magnitude and frequency. They are used extensively in motor drives, active filters, uninterrupted power supplies and UPF controllers in power systems. When variable frequency drives use inverters, a high common-mode voltage is induced producing large CMI (Common mode current) which damages the motor and the electronic equipment present at its outer terminals.

1.2 AC Motors

An AC motor transfers electrical energy into mechanical motion. They are flexible due to their simplicity, reliability and efficiency. AC motors are utilized in a broad variety of applications, from small electric devices in our homes to large machinery in major factories and businesses. It works by regularly switching the direction of the electric current. AC motors employ the back-and-forth flow of power to produce spinning motion. They have two basic parts: a stationary stator and a revolving rotor. They use a stator and rotor to convert AC electricity AC motors are widely utilized in appliances, industrial machinery and other applications due to their high efficiency and adaptability.

1.2.1 Construction of AC Motor

An alternating current (AC) motor is made up of a rotor and a stator which is shown in Figure 1.1. The stator is made up of coils that carry alternating currents, which can generate magnetic fields. As the current alternates, it causes rotation in the rotor resulting in mechanical motion. This basic but effective design powers a variety of devices, including fans, pumps, etc.

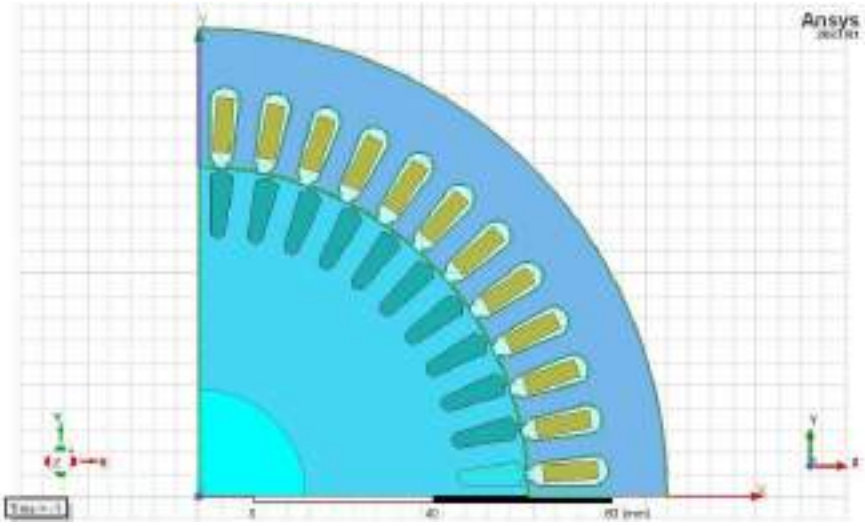

Figure 1.1. 2D Ansys Representation of Stator and Rotor Slots in Induction Motor.

Stator

The stator is the stationary component of the motor. It contains coils that are connected to a power supply. Electricity flows through these coils and generates a magnetic field.

Rotor

The rotor is the moving part of the motor which is located inside the stator. It is often formed of a conductive material, such as copper, and is free to rotate. The stator's magnetic field interacts with the rotor, causing a rotational motion.

Motor Shaft

The motor shaft is a spindle or rod that extends from the rotor. When the rotor rotates owing to magnetic contact, the motor shaft likewise turns. This rotational motion can be utilized for a variety of purposes. The constructive parts of the induction motor are more clearly depicted in Figure 1.2.

Bearings

Bearings are the mechanical components that support and promote a smooth rotation of the motor shaft. They reduce the friction between the motor shaft and housing. Bearings improve the motor's overall efficiency and durability.

Enclosure

The enclosure is the outside casing or housing that contains and protects the motor's internal components. It protects the motor from external contaminants such as dust, moisture and also ensures safety. The cage gives protection against accidental damage due to moving parts.

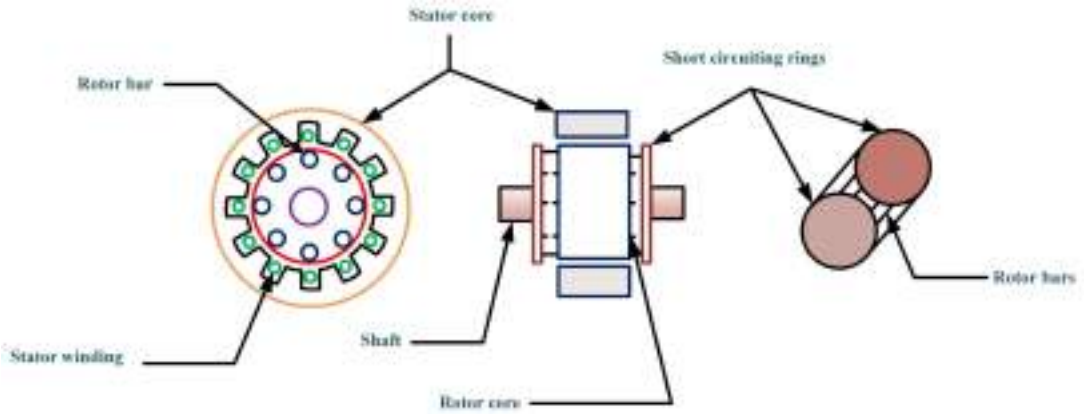

Figure 1.2. Constructive Parts of Induction Motor

1.2.2 Working Principle of AC Motors

Generally, AC motors get their power from an electrical outlet. The motor consists of two primary components i.e. the stator and the rotor. The stator coils transmit an electric

current, resulting in a magnetic field. The rotor, a rotating conductive component, interacts with the stator's magnetic field. This interaction creates a turning force on the rotor, forcing it to rotate around the motor shaft. The motor shaft is used to transfer the rotor's rotating motion. This rotating motor shaft can be used for a variety of purposes, depending on the application. Bearings assist and promote smooth rotation, which improves the motor's efficiency and durability. AC motors are versatile and can be used in a variety of applications like fans, pumps and machines

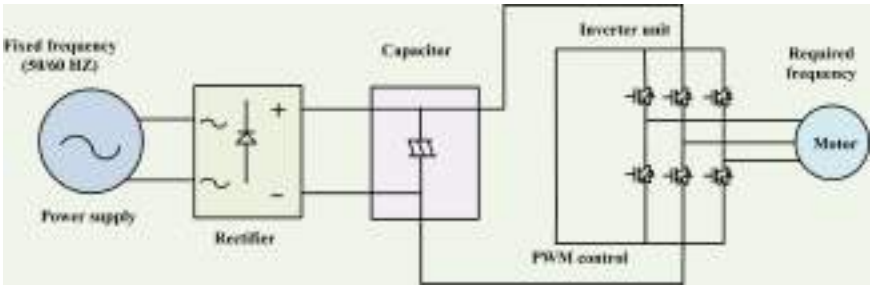

Figure 1.3. Power Electronic Converter fed Induction Motor.

1.2.3 Types of AC Motors

AC motors operate based on transforming electrical energy into mechanical energy. AC motor is widely categorized into two categories, mainly:

1. Synchronous motors.
2. Induction motors.

1.2.4 Synchronous Motor

A synchronous motor is an electrical device that operates at a constant speed while synchronizing with the frequency of the power supply. It is commonly utilized in appliances and industrial gear. The motor's rotor rotates at the same rate as the magnetic field, resulting in precise and efficient functioning in a variety of applications.

1.2.5 Induction Motor

Induction motors are a prevalent form of electric motor. It works on the principle of electromagnetic induction, which transfers electrical energy to the rotor (spinning portion) without requiring a direct electrical connection. Induction motors are widely utilized in a variety of applications because they are dependable and simple to convert electrical energy

to mechanical power. When alternating current electricity is given to the stator, it generates a revolving magnetic field. This magnetic field establishes a current in the rotor. The interaction of the stator and rotor magnetic fields causes the rotor to rotate, driving the mechanical load attached to the motor. Figure 1.4 is an induction motor 3-D view observed in Ansys software.
Induction motors have a wide range of applications, including domestic appliances, industrial machinery, pumps, fans, conveyor systems, household appliances (such as washing machines and refrigerators), blowers for HVAC and ventilation systems, electric vehicles for propulsion, and water pumps for agriculture, irrigation, and household uses.

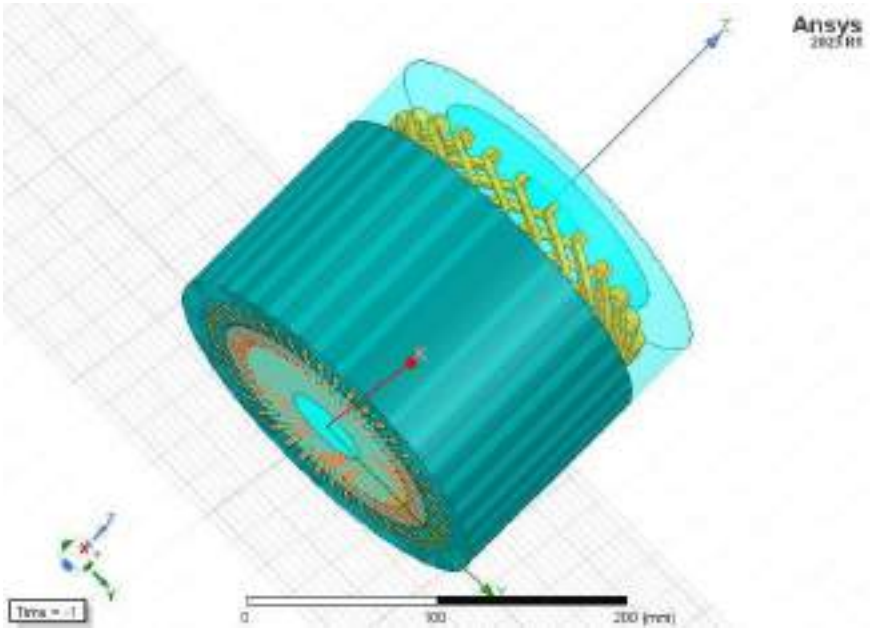

Figure 1.4. Induction motor.

1.2.6 Three Phase Induction Motors

In modern days, particularly three-phase induction motors are often utilized in AC motors to transmit mechanical power. Among all the motors utilized in ventures, three-phase induction motors account for 80%. As a result, the induction motor is the fundamental motor among all other types of motors. Three-phase motors are classified into two types based on the rotor winding (armature coil winding) they are:

1. Squirrel Cage Induction Motor
2. Slip Ring or Wound Type Induction Motor.

1.2.7 Squirrel Cage Induction Motor

This type of rotor appears to be in the same condition as a squirrel's enclosure. It is commonly referred to as an induction squirrel cage motor. It is both simple to produce and long-lasting. Almost 80% of motors are of squirrel cage type. The enclosed center of the rotor is fashioned like a tube, with spaces along the outside borders. The spaces are not comparable and they gradually become distorted. It promotes magnetic locking between the stator and rotor teeth. It produces smooth action. The squirrel cage rotor consists of rotor bars rather than rotor windings. Rotor bars are made of either aluminum, metal, or copper. End rings permanently shorten the rotor bars. This results in a full closure of the rotor circuit. The rotor bars are mechanically supported by welding and are short-circuited by end rings. In this type of rotor, slip rings and brushes are not utilized. As a result, the design of the squirrel cage motor is simpler and more lasting.

Advantages of Squirrel Cage Induction Motor

Squirrel cage motors have a simple and durable design, resulting in smooth and dependable performance. The rotor's closed cage design removes the need for external connections, resulting in less wear and maintenance issues. Squirrel cage motors excel at producing high beginning torque. These motors are affordable and ideal for a variety of modern devices such as pumps, fans and compressors.

1.2.8 Wound Rotor or Slip Ring Induction Motor

Slip-ring induction motors are frequently referred to as wound rotor motors. The rotor is made out of a tube-shaped hub with slots on its outer edges. The rotor winding is put into the slots. In this sort of rotor, the winding is configured so that the number of rotor winding slots equals the number of stator winding poles. The rotor winding might be visualized as a star or a delta. The slip rings are attached to the end terminals of the rotor winding. As a result, it is called a slip-ring induction motor engine.

1.3 Working Principle of Three-Phase Induction Motor

The stator windings are electrically connected at a 120° angle. When a three-phase power source is applied to the stator winding, it induces a rotating magnetic field within the stator circuit. The speed of the revolving magnetic field is referred to as synchronous speed (N_s). According to Faraday's law, EMF is induced based on the rate of change of $\frac{d\phi}{dt}$. The rotor circuit disrupts the stator magnetic field, resulting in an EMF in the rotor bar or winding. As the rotor is the surrounding part, the EMF causes current to flow via

the rotor circuit. The rotor develops a second magnetic field and the rotor tends to rotate. As the rotor tends to rotate, the relative motion between stator flux and rotor flux decreases which can be explained by len's law. Since the inductance generates rotor current, these motors are known as induction motors. The rotor speed is not the same as the synchronous speed. The rotor attempts to obtain the stator's field speed. Nevertheless, it never gets it. As a result, the rotational speed of the rotor is somewhat lower than the synchronous speed.

The slip is zero when the real and synchronous speeds of the rotor match. However, with an induction motor, this scenario is never encountered. This is because at zero slip, both speeds are equal, resulting in no relative movement. As a result, no electromotive force (EMF) is induced in the rotor circuit and the rotor current is zero which makes the motor to stop.

The fundamental advantage of a three-phase induction motor is its self-starting capability, which eliminates the need for additional devices. Its capacity to operate at a consistent speed under variable loads enhances its dependability in practical applications. Furthermore, the absence of brushes in the design of the motor decreases maintenance requirements, contributing to its endurance and longevity.

1.4 Power Electronic Converters

Power electronic devices are a combination of converter and controller, with the converter operating by the control signal supplied by the controller. A power electronic converter consists of power semiconductor devices that are controlled by integrated circuits. The classification of power electronic converters is given in the figure 1.5.

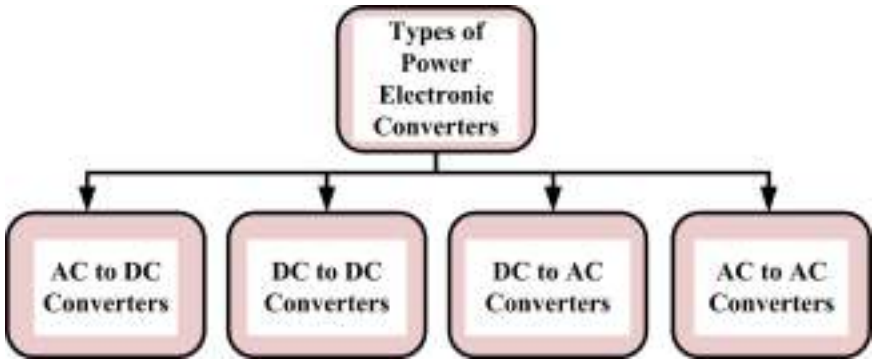

Figure 1.5. Classification of Power Electronic Converters.

AC to DC Converters

AC-DC converters are also called rectifiers which convert an alternating current (AC) signal to a direct current (DC).

DC to DC Converters

Choppers are converters that convert a fixed frequency DC signal at the input to a variable DC signal at the output. The resultant output DC voltage may differ in amplitude from the source voltage. Power transistors, MOSFETs and thyristors are common semiconductor devices utilized in their manufacturing. A low-power signal regulates the output of these semiconductor devices via a control unit.

AC to AC Converters

An AC-AC converters convert a fixed-frequency AC signal into a variable AC output voltage. They are called cyclo converters.

DC-to-AC Converters

Inverters are devices that convert DC signals to alternating current (AC). The applied input is a fixed DC voltage derived from batteries, whereas the output is a variable AC voltage as shown in figure 1.6. The signal's voltage and frequency are changeable. The semiconductor device or thyristor, is turned off using either line, load or forced commutation. Thus, the employment of inverters converts a fixed DC voltage into an alternating current voltage with variable frequency. Power transistors, MOSFETs, IGBTs, GTOs and thyristors are common semiconductor devices utilized. Inverters are primarily used in induction and synchronous motor drives, as well as UPS, aircraft, space power supplies, high voltage DC transmission systems, induction heating supplies, low power mobile systems such as the flashlight discharge system in a photographic camera and in very high power industrial systems. They can be used in both high-power and low-power applications.

Figure 1.6. Energy Flow in DC to AC Converter

1.5 Inverter Controlled Induction Motors

Induction motors are designed to be powered by a constant magnitude AC mains power source with a fixed frequency of 50 or 60Hz. They have grown in popularity since their

inception, owing to the cost and robustness advantages they provide over DC motors as well as the near-complete absence of maintenance requirements. However, when fed with a constant frequency input, their speed is difficult to control. Induction motors are ideal for quasi-fixed-speed operation, which is why DC motors have long been preferred in variable-speed driving applications. To regulate speed, induction motors must be powered by a voltage and frequency-adjustable power supply. The development of modern power electronics has made it possible to build effective static converters that are capable of producing changeable magnitude and frequency AC from DC and voltage input sources. Inverters are the most commonly used devices for this purpose and they use a method called modulation. The constant development in managing inverter output waveforms has been primarily attributed to improved modulation techniques, beginning with the well-known sine-triangle technique created a few decades ago and progressing to the space vector modulation techniques used today. Inverters are classified into two types: voltage-source, which generates AC voltage outputs and current-source, which generates AC current outputs. The theoretical analysis of voltage-source and current-source inverters can be treated similarly, but the practical implementation of the two circuits as well as the specifics of their control systems are very different.

An inverter adjusts the frequency of power supplied to an alternating current motor to control the motor's spinning speed. Without an inverter, the AC motor would start at full speed as soon as the power supply was turned on. It would be unable to alter the speed, which would limit the motor's applications. The use of an inverter to alter the speed and acceleration of an AC motor expands its variety of applications as compared to a motor that operates at a constant speed. The power flow in an electric drive system is depicted in figure 1.7. A motor's speed is often measured in terms of revolutions per minute (rpm). The acceleration rate is defined as the change in speed over a certain amount of time.

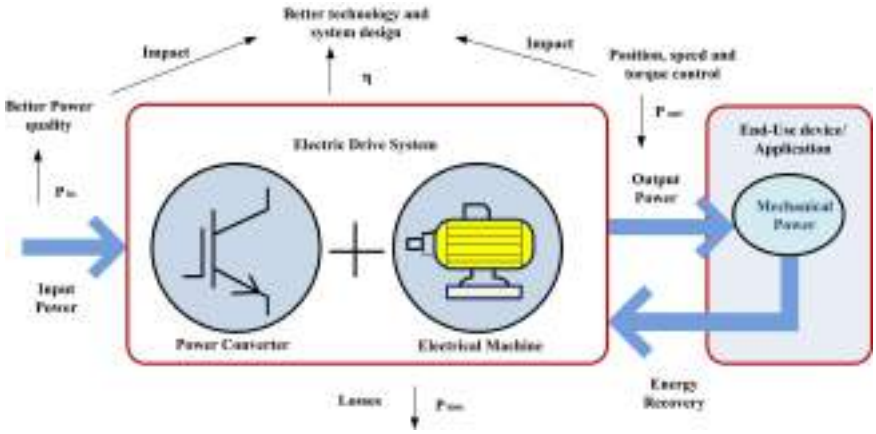

Figure 1.7. Power Flow in an Electric Drive System

Freely Set and Change AC Power Frequency and Voltage

An inverter uses this feature to freely control the speed and torque of a motor. This sort of control, in which the frequency and voltage can be freely adjusted, is known as pulse width modulation or PWM. The inverter's voltage output is in pulse form. The inverter generates a pulsed voltage which is smoothed by the motor coil, resulting in a sine wave current that goes to the motor which controls its speed and torque. These inverters power the IM while boosting the operation's safety and dependability, but they also increase harmonic frequency traces. The PWM modulation technique and switching frequency define the harmonic amplitudes and wide-band frequencies. PWM-controlled inverters used with *WBG* devices such as *SiC* (Silicon Carbide), *GaN* (Gallium Nitride), *GaAs* (Gallium Arsenide), *AlN* (Aluminum Nitride) and others have crucial switching frequencies ranging from a few KHZ to tens of KHZ. Aside from increasing the harmonic content at the inverter's output terminal, they also generate a high-frequency common-mode voltage (CMV) which is a severe issue in switching power converter-fed IM. This occurs with the shaft voltage which generates bearing current via the AC machine's stray capacitive and inductive linked channels. High modulation frequency reduces lower-order harmonics while increasing the inverter's loss. These lower-order harmonics are harmful to motors because they generate torsional oscillations, pulsing torques in the shaft and rotor bar breakage. Research is being carried out to protect the motor from these problems.

1.6 Problem Setting

As we use different PWM techniques to control the switching of the inverters, the common mode voltage problem is invoked in the drives. The magnitude and frequency of CMV depend on various PWM techniques used. This CMV induces shaft voltage on the rotor side. When the shaft voltage exceeds the breakdown voltage of the lubricant of bearings, there flows a current in the bearings. It also disturbs the power of electronic equipment connected to the motor. Thus, the motor starts to malfunction. To reduce CMV many hardware and software solutions are being proposed . In a conventional three-phase two-level drive system different BUS clamping techniques have been performed to reduce the CMV. A comparative analysis is performed among conventional SVPWM, 30° , 60° , 120° , 240° BUS clamped SVPWM techniques. Out of which, the 240° bus-clamped PWM technique produces the least common mode voltage in a three-phase, two-level inverter-fed VSI. Both multi-level and multi-phase systems provide a greater degree of freedom to control CMV over conventional three-phase two-level systems. Multi-level and Multi-phase systems offer inherent fault tolerance capability for some machine failures, high power density, high efficiency, more reliability and lower costs. Multi-phase machines reduce the

total power per phase and also torque ripple. THD value will be reduced due to the reduction of harmonic components. More redundancies are available in switching to minimize CMV The main motto of this work is to reduce the CMV in conventional 2-level VSI using bus clamping methods and by comparing its various performance parameters. Further, the work is being progressed towards the multi-level and multi-phase configurations which provide more flexibility in reducing CMV and reducing the THD ensuring good torque profile. An algorithm to reduce the instantaneous CMV in three-phase, three-level VSI is simulated. This can further be easily extended to poly-phase and multi-level with lesser hardware.

1.7 Thesis Outline

Chapter 1 This chapter explains the AC motors, their construction, working principle and classification. It further explores more on induction motors and their types. Power electronic equipment controlling induction motor is detailly classified and the control of inverter fed induction motor is explained.

Chapter 2 This chapter includes research on the publications that describe the CMV formation and its various CMV-reducing techniques. Multi-phase and multi-level inverter topologies are also explored.

Chapter 3 This chapter explains the concept of formation of common mode voltage. The formation of CMCI and CMV is explained in detail and bearing current generating mechanisms are pointed. Capacitance effects are represented in the equivalent circuit.

Chapter 4 Mathematical modeling of a three-phase induction motor is derived in this chapter. Voltage equations of the stator and rotor are represented in the D-Q frame.

Chapter 5 This chapter shows the work of the various bus clamping PWM techniques in a conventional 2-level inverter. It explores different bus clamping techniques and compares their performance parameters with the 240° clamping method. It proves that the CMV is drastically reduced as the clamping is increased.

Chapter 6 This chapter explains the importance of multi-level inverters and their classification of various topologies. Further it works on CMV-reducing techniques like a double-modulating wave and CB-PWM to reduce instantaneous CMV in a three-level three-phase induction motor.

Chapter 7 This chapter describes the importance of multi-phase drive systems and explores five-phase systems. It shows the mathematical modeling of five-phase and the various PWM techniques like PD-PWM and POD-PWM to reduce the common mode voltage and maintain the THD and torque profiles.

Chapter 2

LITERATURE REVIEW

2.1 Introduction

SiC - MOSFETs excel over Si - IGBTs in terms of frequency and power density, making them ideal for variable-speed motor drives in electric vehicles (EVs). However, because of their fast switching speed and frequency, SiC MOSFETs are likely to have some disadvantages, such as a higher common mode voltage (CMV). The usage of a PWM inverter produces some high-frequency CMV, which causes Electromagnetic interference (EMI) in the drive system and also shaft voltage due to the coupling effect of high-frequency parasitic capacitances. Therefore as the advancement goes to the usage of high-frequency switches, it is important to mitigate CMV and improve the drive's performance. Bearing currents and the induced shaft voltage are the major factors resulting in almost 9% of bearing failures. These bearing currents result in significant damage to the mechanical parts of the motor. Common mode voltage (CMV) is one of the major causes of the production of bearing currents. Research has been conducted on how the common mode voltage is produced and the effects of it on the drive system. A lot of hardware as well as software solutions have been proposed to reduce this common mode voltage and still the research is being continued towards the multi-level and multi-phase topologies.

2.2 Litrature Review

"Motor Bearing Current Phenomenon and 3-Level Inverter Technology."– YASKAWA-A product Application note June 22, 2005. This note detail describes the causes of the common mode voltage and its effects. It shows the clear classification of bearing currents and also the various capacitance effects that contribute to the common mode voltage. It gives a comparison between 2-level and 3-level inverter topologies and highlights their CMV magnitudes. It mentions the various reduction techniques and finally focuses

on CMV reduction using a 3-level inverter. “Triangle-Comparison Approach and Space Vector Approach to Pulsewidth Modulation in Inverter Fed Drives.” - G. Narayanan and V.T. Ranganathan - IISC_journal – September 2000. This research examines the equivalence of two famous approaches to Pulsewidth Modulation (PWM) in induction motor drives: the triangle-comparison approach and the space vector approach. It identifies the conditions under which they are equal. It demonstrates that the space vector approach is more general and provides more degrees of freedom than the triangle-comparison approach. “Common-Mode Reduction SVPWM for Three-Phase Motor Fed by Two-Level Voltage Source Inverter.” - Jian Zheng, Ming Cheng Lyu, Shengqing Li, Qiwu Luo and Keyuan Huang. - Energies 2020, 13(15), 3884. This paper investigates the CMRSVPWM (Common Mode Reduction SVPWM) technique to lower the CMV magnitude and frequency in a three-phase motor fed by 2-level VSI. It compares conventional SVPWM with CMRSVPWM commenting on the torque profile, speed response, and THD. CMV magnitude in CMRSVPWM is reduced by 66.67% compared to CSVPWM.

“Common-Mode Voltage Elimination in Multilevel Power Inverter-Based Motor Drive Applications.” Endlika Robles, Markel Fernandez, JORDI ZARAGOZA, IÑIGO MARTINEZ DE ALEGRIA and JON ANDREU.- IEEE Access 10.1109/ACCESS.2021.3137892. This paper explains the importance of multi-level inverters in reducing the common mode voltage. It investigates the most recent topologies of multi-level inverters and evaluates their performance. It explains the flexibility of using redundant states in reducing CMV. It comments that the ZCMV-PWM (Zero Common Mode Voltage-PWM)technique is the most advantageous technique among all the CMV-reducing techniques ensuring good performance both in terms of CMV and in its balance between power losses, signal quality, and linear range. It gives 100% elimination of CMV. “Comprehensive Analysis and Experimental Validation Of 240 degree – Clamped Space Vector PWM Technique Eliminating Zero States For EV Traction Inverters With Dynamic DC Link.” - Deliang Wu, Hafsa Qamar and Rajapandian Ayyanar - IEEE Transaction on Power Electronics, 2020. This paper explains the cascaded connection of the dc-dc stage and dc-ac stage allowing the dc link to be dynamically variable which is a suitable application for EV. It compares various bus clamping methods with conventional SVPWM. It explains a new type of clamping called the 240-degree clamping concept and shows the reduction in common mode voltage by using this method. It also explains the importance of dynamic DC link voltage and its application in EVs.

“Performance Evaluation of Various Bus Clamped Space Vector Pulse Width Modulation Techniques.” Meenu D. Nair , Jayanta Biswas, G. Vivek, and Mukti Barai -Journal of Power Electronics, Vol. 17, No. 5, pp. 1244-1255, September 2017. This paper describes various bus clamping techniques and calculates the weighted THD of all the bus clamping methods. It analyzes the performance parameters at different modulation indices and plots

the graphs.

“Effects of Switching Frequency and Motor Speed on Common Mode Voltage, Common Mode Current and Shaft Voltage in PWM Inverter-fed Induction Motors.”- T. G. Arora, M. M. Renge and M. V. Aware - This paper explains the effects of switching frequency and speed of the motor on the CMV, shaft voltage and CMI. Common mode current peak factor, Shaft voltage peak factor and Common mode voltage peak factor are calculated which indicate the stresses generated on ground wall insulation of the motor and bearings. This helps in analyzing the life of the motor.

“Performance Analysis of Multi-Carrier PWM and Space Vector Modulation Techniques for Five-Phase Three-Level Neutral Point Clamped Inverter.”- VINOTH JAYAKUMAR AND JOSIAH LANGE MUNDA 1, BHARATIRAJA CHOKKALINGAM 1,(Senior Member, IEEE), 2,(Member, IEEE)- April 5, 2022, IEEE Access. This paper explains about importance of multi-phase and multi-level inverters. It describes various multi-carrier PWM techniques like PD, POD and APOD techniques with experimental setup. SVM is being used to obtain significant performance parameters like THD, DC link balancing and CMV in all these techniques. “A CB-PWM Technique for Eliminating CMV in Multilevel Multiphase VSI.”- Abanishwar Chakrabarti, Member, IEEE, Koustuv Sarkar, Student Member, IEEE, Prabir Ranjan Kasari, Member, IEEE, Bikram Das, Senior Member, IEEE, and Sujit K. Biswas, Senior Member, IEEE.- IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 70, NO. 9, SEPTEMBER 2023. This paper explains the algorithm to reduce the instantaneous CMV to almost zero by using virtual level concept. There is more scope to extend it to multi-phase and multi-level topologies.

Chapter 3

COMMON MODE VOLTAGE FUNDAMENTALS

3.1 Introduction

This chapter will provide an overview of generation common mode voltage (CMV) and its causes. Using a common mode equivalent circuit, the impact of CMV on AC motors will be examined. This chapter will examine the current techniques for reducing CMV. In recent decades, the CMV generated by VSIs has been the focus of extensive study. Shaft voltage and subsequently bearing currents are caused by the CMV. In addition to excess voltage stress on the motor windings, there occurs an insulation breakage. Additionally, sensitive control electronics that are situated close to common-mode noise channels may experience electromagnetic interference (EMI) from the CMV and induced common-mode currents (CMI's).

3.2 Theory of Common Mode Voltage (CMV)

It has been noted that the capacitance effects are present between stator winding to stator frame (C_{wf}), stator winding to rotor capacitance (C_{wr}), rotor to frame capacitance (C_{rf}), phase to phase capacitance (C_{ph}) and bearing capacitance (C_b). The equations for bearing current and circulating current [1] are respectively given by:

$$i_b = C_b \cdot \frac{dV_b}{dt} \tag{3.2.1}$$

$$i_{wf} = C_{wf} \cdot \frac{dV_{sg}}{dt} \tag{3.2.2}$$

It is noted that CMV is responsible for three primary bearing currents which are represented in Figure 3.4.

- A current known as electrostatic discharge machining, or EDM, happens when the bearing voltage V_b rises above a minimum value. It generates an EDM current pulse and causes lubricant to break down as a result of elevated temperatures
- High $\frac{dV_b}{dt}$ causes a capacitive bearing current of i_b.
- Circulating current due to high $\frac{dV_{sg}}{dt}$.

3.3 CMV and its Effects in AC Motor Drive Systems

In any balanced AC three-phase motor system with fully sinusoidal excitation, the phase voltages with respect to the motor's neutral point (assuming a Y connection) are made up entirely of positive sequence components, therefore the instantaneous sum of the time-domain phase voltages is zero. This circumstance typically applies to motors that are directly linked to the utility mains. The main disadvantage of this scenario is the inability to manage the motor speed and torque, which results in sub-optimal control and operational efficiency. Furthermore, direct-line starting can result in inrush currents that are more than six times the motor's rated current.

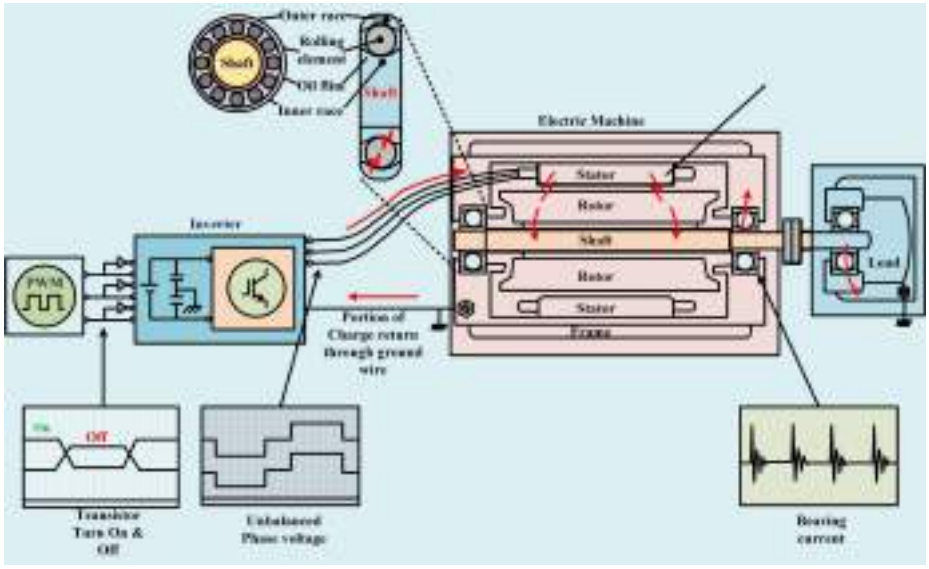

Figure 3.1. Generation of Bearing Currents.

Using VSI-based *ASDs*, whether two-level or multilevel solves these problems but they have significant drawbacks because the output voltages that they produce are not sinusoidal and their time-domain phase voltages at any instant during the ac cycle may not total to zero. VSIs use high-speed switching devices, such as insulated gate bipolar junction transistors (IGBTs) or metal-oxide field-effect transistors (MOSFETs) to accomplish DC-AC

power conversion by generating an AC output from a DC source. Unlike sinusoidal ac sources, the VSI produces rectangular pulses with a rapid change in output voltage with respect to time $\frac{dV}{dt}$ during switching transitions, waveforms shown in Figure 3.1.In motor driving applications, the load of the VSI is mostly inductive. However, parasitic capacitances across the system are unavoidable. In the ac component of the drive system, the parasitic capacitance between phases contributes to induced differential mode current (*DMI*) as a result of the switching devices high differential-mode (*DM*) $\frac{dV}{dt}$ values. Similarly, the parasitic capacitance between each phase and the system ground contributes to the induced CMI caused by the switching devices high CM $\frac{dV}{dt}$.

The $\frac{dv}{dt}$ produced by each switching device normally which is in the range of 5 $\frac{kV}{\mu s}$ to $15\frac{kV}{\mu s}$, is an important measure. It is solely responsible for the common mode charging and discharging impulse currents produced by the parasitic capacitances between the system ground and motor windings, cables, inverter and semiconductors. The induced CMIs return to the power mains via multiple ground routes, as illustrated in Figure 3.3. When the inverter operates under PWM conditions rather than six-step (two-level inverters), twelve-step (three-level inverters) and so on the frequency of the CMI's rises to values around the carrier frequency (2-20 KHZ) and multiples. Parasitic resonance can produce high-frequency oscillations ranging from 50 to 300 KHZ. There have been significant scientific attempts to reduce CMIs, however the primary focus of this thesis is to mitigate/eliminate CMV which significantly lessens CMI.

3.4 Mathematical Derivation of CMV

Inverter pole voltages (output voltage) can be expressed as three-phase output voltages with respect to 'O' [2] or the middle point of the DC bus which can be expressed by:

$$V_{ao} = V_{an} + V_{no} \tag{3.4.1}$$

$$V_{bo} = V_{bn} + V_{no} \tag{3.4.2}$$

$$V_{co} = V_{cn} + V_{no} \tag{3.4.3}$$

Solving for V_{no} gives

$$V_{no} = (V_{ao} + V_{bo} + V_{co} - V_{an} - V_{bn} - V_{cn})/3 \tag{3.4.4}$$

when the load is balanced all the phase to neutral voltages will be equal and sum up to 0. Finally, the CMV can be derived as [3] :

$$V_{no} = (V_{ao} + V_{bo} + V_{co})/3 \tag{3.4.5}$$

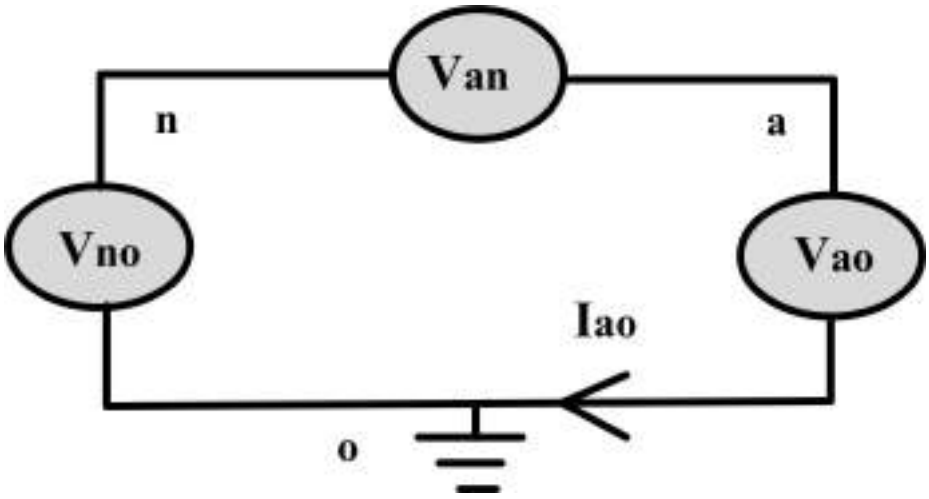

Figure 3.2. Equivalent Circuit of CMV

Many scientists refer to V_{no} as the system's CMV; however, this only holds if the DC bus voltage is balanced in the middle. The potential between the load's neutral point and system ground is known as the CMV and it is important for the load's integrity, as it affects shaft voltages and bearing current [1].

$$V_{ng} = (V_{ao} + V_{bo} + V_{co})/3 \tag{3.4.6}$$

This CMV in Equation is composed of high frequency common-mode pulses.

3.5 Common Mode Current Generating Mechanisms and The Bearing Currents:

To analyze the CMI generating mechanisms and CMI routes, the common mode equivalent circuit of a three-phase induction motor should be examined. As seen in the Figure 3.3, capacitive routes exist between the motor windings and the ground, which are particularly effective at high frequencies. The resistance of the cable and the inductance of the motor windings can be ignored in the CM equivalent circuit. In the equivalent circuit Figure 3.5 stray capacitances between the stator winding, rotor and motor frame are illustrated separately. Of these capacitances, C_{wf} which is the equivalent capacitance between motor windings and motor frame which is significantly higher than other capacitances. Therefore, the motor common mode equivalent capacitance (C_{eq}) can be assumed as equal to the C_{wf}. C_{wr} is the capacitance between the stator windings and rotor,C_{rf} is the capacitance between the rotor and motor frame (excluding bearing capacitance) and C_b is the bearing capacitance. Since there are two bearings in each motor C_b is multiplied by 2 in the equivalent model.

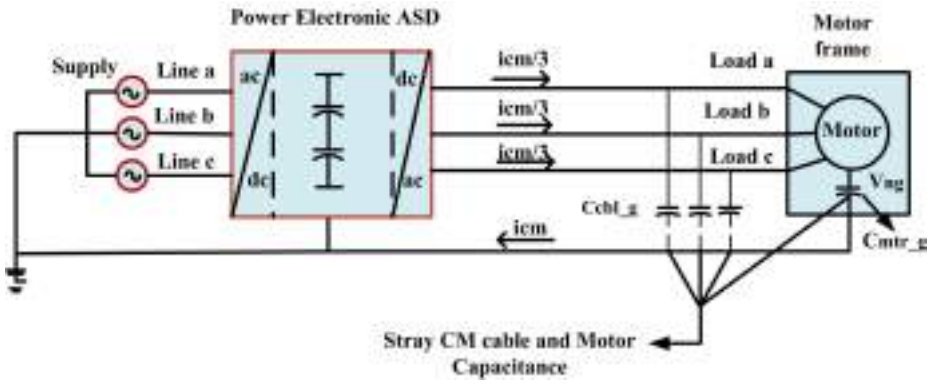

Figure 3.3. Source_Drive_Motor Simplified Circuit Showing Motor Cable and Motor.

i_{cm} is the overall leakage current flowing from the motor frame to the ground (CMI) and i_b is the bearing current. In practice bearing currents compose a very little fraction of the overall leakage currents. However, they are extremely dangerous since they cause bearing failures. Bearing currents are classified into numerous sorts based on their generation method Figures 3.4 categorizes inverter-induced bearing currents based on their cause.

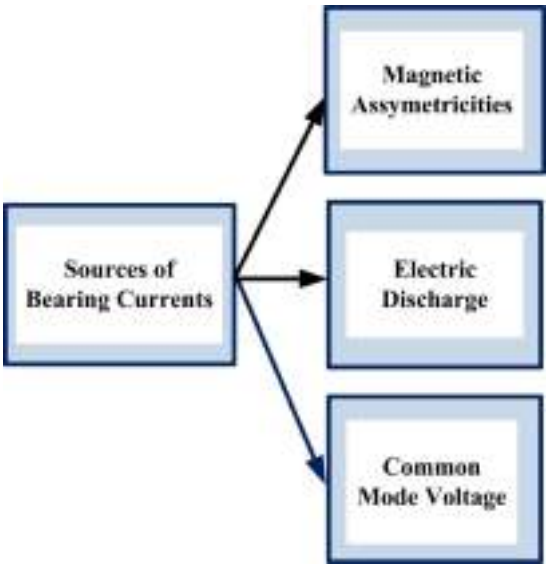

Figure 3.4. Classification of Bearing Currents

The CMV produces capacitive bearing currents, electric discharge machine (EDM) bearing currents, and leakage currents. The magnitude of the CMV is effective for generating EDM bearing currents, whereas the magnitude and $\frac{dV}{dt}$ of the CMV are effective for generating capacitive bearing currents and leakage currents respectively. The leaking ground currents cause rotor ground currents and High Frequency (*HF*) shaft voltage, which is the source of HF circulating bearing currents. Among these forms of bearing currents, capacitive bearing currents are small in magnitude and harmless. The rotor ground currents may be

harmful but they occur only in operation where the rotor is grounded (via the mechanical load). Therefore, the EDM and the HF circulating bearing currents are most important. EDM bearing currents come from voltage buildup over the bearing (bearing voltage or shaft voltage). The motor common mode equivalent capacitance values determine the bearing voltage ratio (*BVR*), which is described as

$$BVR = C_{wr}/(C_{wr} + C_{rf} + C_b) \tag{3.5.1}$$

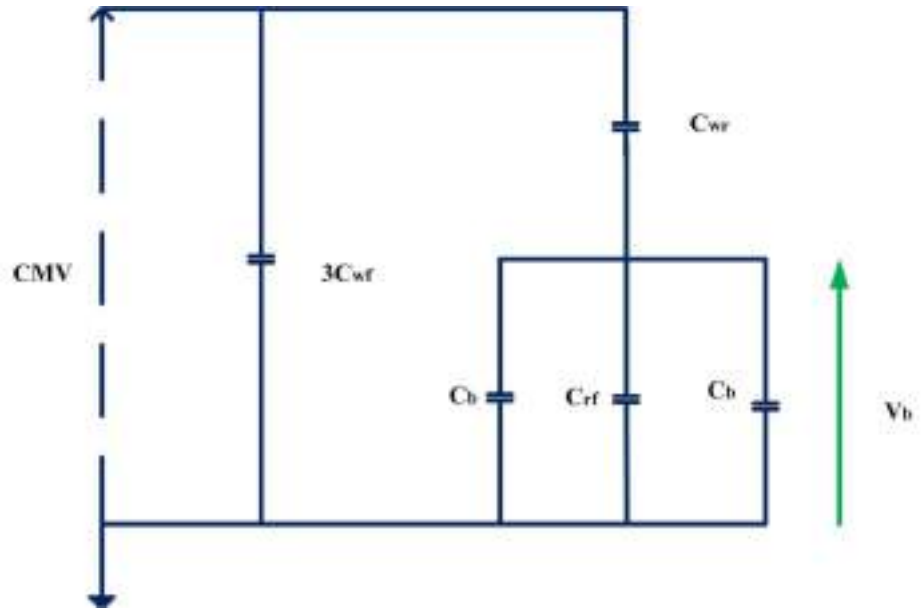

Figure 3.5. Equivalent Circuit of Motor Capacitances.

In actuality, $C_{rf} > C_{wr}$ hence *BVR* often ranges between 2% and 10%. Since the grease film thickness is a fraction of μm, discharges often occur when the bearing build-up voltage approaches several volts. When an electrical discharge occurs, a rapid current pulse is produced, and the bearing voltage abruptly drops to zero. During the breakdown instant, the CMV waveform shows a steep fall or rise. The size of the breakdown current depends on the bearing voltage before discharge. Discharges are widespread in low-quality bearings with rough surfaces. However, because discharges occur at relatively low built-up bearing voltages, the magnitudes of the bearing current impulses are relatively lower. EDM bearing currents are lower at low motor speeds ($<$ 100 rpm) due to metallic contact inside the bearing, which prevents voltage buildup. The motor size dependency of the EDM-bearing currents is negligible. As a result, for small motors (few KW or less), EDM bearing currents are high and effective relative to the motor size. In small motors, almost all bearing currents are EDM-type bearing currents, because HF circulation bearing currents are only

effective at extremely high-power motors (100 kW and higher). As the motor size increases, the contribution of EDM-bearing currents diminishes. Leakage currents flowing from the motor windings to the ground cause the currents measured at two opposite ends of a phase winding coil to be unequal. These imbalanced currents provide a net flux inside the motor, which induces HF circulation currents. These currents run inside the motor and through the bearings, harming them. HF circulation bearing currents are dominating at low speeds, particularly in big motors. The densities (J_b) of the bearing currents, in addition to their magnitudes are crucial because they scale the danger of bearing failure. As the motor size increases the bearing currents also increases. However, if the increment of the bearing current is less than the increment of the bearing surface, the bearing failures occur less likely. In small motors (less than a few KW), EDM-type bearing currents are dominant, resulting in extremely high bearing currents relative to the motor size. In small motors, as the motor size and power increase in size, bearing currents will increase but the increase is relatively limited since the EDM bearing currents have a low dependency on motor size. As a result, when motor size increases, J_b drops until the HF circulation bearing currents become dominant. Therefore in motors between 10kW and 100kW, J_b is rather low since neither EDM nor HF circulating bearing currents are prominent. Above 100kW, HF circulating bearing currents are dominant and their magnitudes increase considerably with motor size, therefore J_b increases.

Chapter 4

MODELING OF THREE-PHASE INDUCTION MOTOR

4.1 Introduction

Nowadays, induction motors have become the dominant machines in industries due to their better speed control. To obtain the dynamic speed response induction motors require variable voltage variable frequency supply which can be obtained by using PWM techniques. PWM techniques play a very important role in the speed control of induction motors. Due to the rapid advancement in fast-switching semiconductor devices, electric drives have been becoming more popular. In the past few days, separately excited DC motors have played a vital role in various applications because of their decoupling nature of torque and flux. But due to their high maintenance, high weight-to-volume ratio and commutation issues, these motors are least preferred now. AC drives replace these DC motors by providing wide control over output voltage and frequency. They have robust construction and least maintenance.

4.1.1 Mathematical Modeling of Three-Phase Induction Motor

Modeling of any physical system is necessary in the research field because it allows researchers to predict how the system can be improved against various phenomena and thus learn more about the mechanisms that control it. The induction machine can be modeled by different methods, depending on the desired purposes [4].

4.1.2 Three-Phase Model of Induction Motor

The induction motor especially three-phase induction motors are widely used AC motors to produce mechanical power in industrial applications. A three-phase induction motor is a type of AC induction motor that operates on three three-phase supplies as compared to the single-phase induction motor where a single-phase supply is needed to operate it. The

three-phase supply current produces an electromagnetic field in the stator winding which leads to generating torque in the rotor winding of the three-phase induction motor having a magnetic field.
An induction motor looks like complex to analyze because of its winding distribution and geometry. To take exact configuration some of the assumptions are to be made:

Assumptions

1. The air gap is considered as constant
2. The self-inductances are constant.
3. Notching effect is neglected
4. Negligible ferromagnetic losses.
5. Constant permeability.
6. Invariant stator and rotor resistances.
7. Motor is symmetrical.
8. Sinusoidal steady state conditions
9. Saturation is neglected.

To ensure a continuous operation, the induction motor speed must be lower than the synchronous speed, indicating the slip value as positive.

4.1.3 Voltage Equations

Equations of Stator and Rotor Voltages in D-Q Frame

By using park transformation stator and rotor voltage equations can be represented in the rotating frame as:

$$V_{ds} = R_s \cdot I_{ds} + \frac{d\lambda_{ds}}{dt} - \omega \cdot \lambda_{qs} \tag{4.1.1}$$

$$V_{qs} = R_s \cdot I_{qs} + \frac{d\lambda_{qs}}{dt} - \omega \cdot \lambda_{ds} \tag{4.1.2}$$

$$V_{dr} = R_r \cdot I_{dr} + \frac{d\lambda_{dr}}{dt} - (\omega - \omega_r) \cdot \lambda_{qr} \tag{4.1.3}$$

$$V_{qr} = R_r \cdot I_{qr} + \frac{d\lambda_{qr}}{dt} - (\omega - \omega_r) \cdot \lambda_{dr} \tag{4.1.4}$$

In this V_{ds}, V_{qs},V_{dr},V_{qr} are the stator and rotor voltages in d-q frame. Where R_s, R_r are stator and rotor resistances respectively, ω, ω_r are the angular speeds of stator and rotor magnetic fields.

Flux Linkage Equations

The flux linkages can be given as:

$$\lambda_{ds} = L_s \cdot I_{ds} + L_m \cdot I_{dr} \tag{4.1.5}$$

$$\lambda_{qs} = L_s \cdot I_{qs} + L_m \cdot I_{qr} \tag{4.1.6}$$

$$\lambda_{dr} = L_m \cdot I_{ds} + L_r \cdot I_{dr} \tag{4.1.7}$$

$$\lambda_{qr} = L_m \cdot I_{qs} + L_r \cdot I_{qr} \tag{4.1.8}$$

Where L_s, L_r are stator and rotor inductances and L_m is the mutual inductance.

Torque Equation

The mechanical parameters of the motor can be given as:

$$J \cdot \frac{d\omega_r}{dt} = T_e - T_l + B \cdot \omega_r \tag{4.1.9}$$

where J is moment of inertia, B is the damping coefficient, T_e and T_l are the electromagnetic and load torques respectively. This model provides a framework for studying and simulating the performance of a three-phase induction motor under various operating situations. These equations are often solved using numerical simulation tools such as MATLAB/Simulink.

Chapter 5

BUS CLAMPING PWM TECHNIQUES to REDUCE CMV

5.1 Introduction

Voltage source inverters are widely used in medium and high-power applications. Different PWM approaches are utilized in Voltage Source Inverter fed induction motor drives to generate variable voltage and variable frequency 3-phase alternating current. The effective control of inverter output voltage produces desirable results in drives and other applications. PWM approaches have a significant impact on the inverter output. One of the most used ways for controlling inverter switching is space vector pulse width modulation (SVPWM). The space vector pulse width modulation (SVPWM) approach is a common PWM method for medium voltage drive applications. The two most commonly used SVPWM approaches are conventional SVPWM (CSVPWM) and bus-clamped SVPWM (BCSVPWM).

5.2 Conventional 2-Level Inverter

In low-power applications, two-level voltage source inverter (VSI) fed three-phase alternating current induction motors are commonly employed. Figure 5.1 depicts the conventional topology of a three-phase VSI [3]. It has three inverter legs, two switches in parallel, and a freewheel diode per switch. The bipolar approach allows the outputs of each leg to be easily connected to either the upper or lower DC buses.
A three-phase two-level inverter contains 8 switching vectors. The number of switching states can be calculated by using m^n, where m is the number of levels and n is the number of phases. As a result, 2^3= 8 switching vectors [5] are derived and defined in Table 5.1. With free wheel diodes, the output voltage of an inverter leg can be clamped to the DC bus based on the current direction. The basic space vector diagram of a conventional inverter is shown in Figure 5.2.

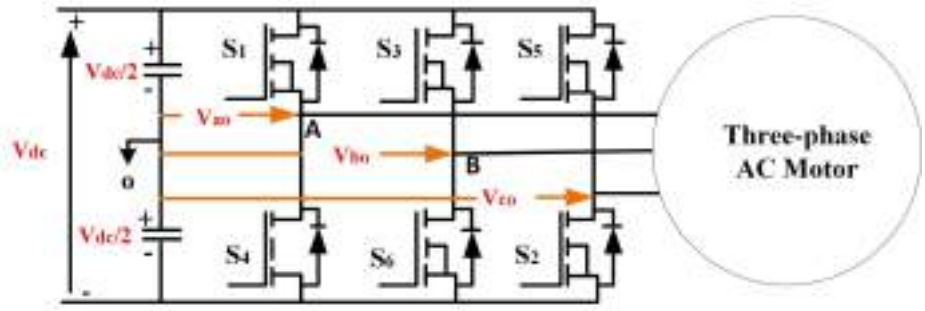

Figure 5.1. Three-Phase Two-Level Inverter.

Space vector		Switching States	On state Switches	Vector Definition
Zero vector	V_0	111 ; 000	S_1,S_3,S_5 ; S_4,S_6,S_2	0
Active vector	V_1	100	S_1,S_6,S_2	V_1=$\frac{2}{3}\cdot V_{dc}\cdot e^{j0}$
	V_2	110	S_1,S_3,S_2	V_2=$\frac{2}{3}\cdot V_{dc}\cdot e^{j\frac{\pi}{3}}$
	V_3	010	S_4,S_3,S_2	V_3=$\frac{2}{3}\cdot V_{dc}\cdot e^{j\frac{2\pi}{3}}$
	V_4	011	S_4,S_3,S_5	V_4=$\frac{2}{3}\cdot V_{dc}\cdot e^{j\frac{3\pi}{3}}$
	V_5	001	S_4,S_6,S_5	V_5=$\frac{2}{3}\cdot V_{dc}\cdot e^{j\frac{4\pi}{3}}$
	V_6	101	S_1,S_6,S_5	V_6=$\frac{2}{3}\cdot V_{dc}\cdot e^{j\frac{5\pi}{3}}$

Table 5.1: Switching definition of Two-Level Inverter

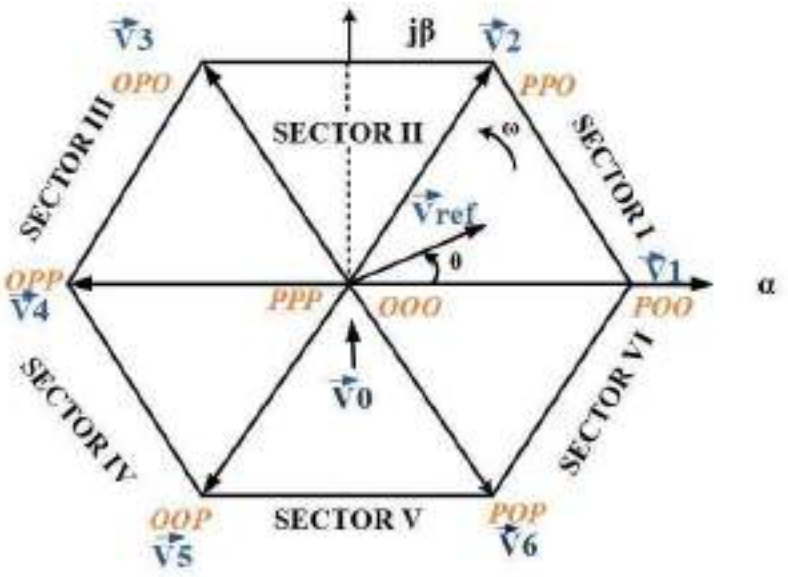

Figure 5.2. Sector Representation for a 2-Level Inverter.

5.3 Bus Clamped PWM Techniques

Modulation techniques are utilized to provide high-quality inverter output voltages and currents for a variety of loads. Several modulation strategies have been presented to achieve the objectives of a wide linear modulation range, low switching loss and better overall inverter efficiency. SVPWM is a popular PWM algorithm for low switching frequency. It achieves higher DC bus utilization by lowering harmonic distortion and switching loss. Different SVPWM switching sequences have been developed to realize the reference vector utilizing the SVPWM approach. The flexibility in the positioning of the zero space vector produces either a continuous or discontinuous SVPWM. Bus clamping approaches use discontinuous space vectors to reduce switching losses and current harmonics. There is a type of PWM approach in which every phase is clamped for 60° in each half cycle, with only the other two phases cycling at that time. The 60° clamping time might be anywhere between the middle 120° of the half cycle. The clamping period can also be broken into smaller intervals. These techniques are known as bus-clamped PWM techniques. This study demonstrates how these PWM approaches can be used to reduce one or more of the following:

1. Switching frequencies and losses.
2. Common mode voltage
3. Total Harmonic Distortion (THD) of Motor Current
4. Computational burden.

The PWM approach used has a direct impact on motor current distortion, torque pulsation, inverter losses, drive efficiency and other factors. The major issue varies according to the power level, device technology and application. There are two popular techniques for implementing real-time PWM: triangle-comparison and space vector. The triangle-comparison approach generates 3-phase PWM waveforms by comparing suitable 3-phase modulating waves to triangular carriers, as in sine-triangle PWM. The reference in the space vector approach is presented as a revolving space vector, as illustrated in Figure 5.3. The reference vector is sampled once every subcycle (T_s), and an average vector equal to the sampled reference vector is obtained for the given subcycle by time-averaging the inverter's distinct vectors. Both ways can generate bus-clamped PWM [5].

The switching frequency-to-fundamental frequency ratio is an important limitation when designing or using PWM schemes. Depending on the power level and technology employed, the switching frequency can range from 5 to several 100 times the fundamental frequency. The investigation of bus-clamped approaches is conducted across a wide range

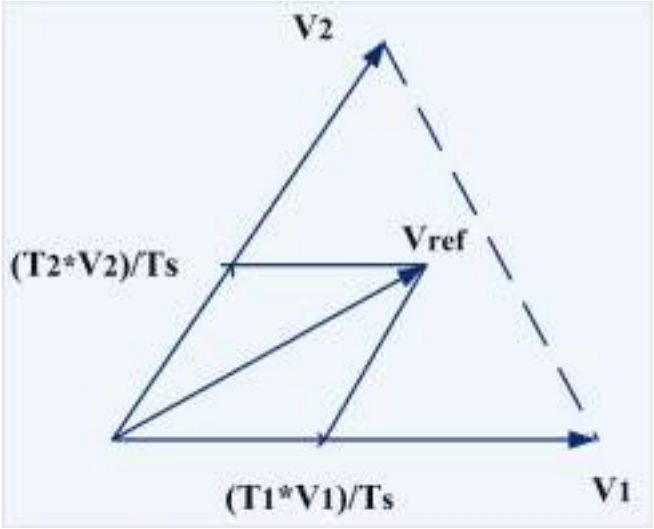

Figure 5.3. Reference vector representation in sector 1.

of switching frequencies. High switching frequencies are those that are larger than or equal to 21 times the fundamental frequency whereas switching frequencies less than 21 times the fundamental frequency are considered low.

The positioning of the zero space vector is flexible, resulting in either continuous or discontinuous SVPWM. Bus clamping approaches utilize discontinuous space vector algorithms to reduce switching losses and current harmonics. During a line cycle, the bus clamping techniques clamp each phase to either the positive or negative DC rail for 120°. The orientation of the desired reference voltage determines the clamped leg and clamping duration. The most well-known clamping methods for BCSVPWM are 60° and 30°. In terms of spectral performance, the BCSVPWM outperforms the CSVPWM in higher modulation indexes [5, 6]. BCSVPWM methods, which clamp a phase to either the positive or negative DC rail, can considerably reduce switching loss. In theory, clamping the phase with the highest current can minimize switching loss by half when compared to CSVPWM. Using the freedom of the zero state division, numerous bus clamping SVPWM algorithms can be generated. The performance of these various SVPWM systems is primarily influenced by the total harmonic distortion factor of the no-load current (*ITHD*) and switching loss. The current harmonic distortion is determined by the switching frequency and PWM method . The harmonic distortion in the motor phase currents must be minimized for the motor drive to function properly [11]. The motor's no-load current factor (*ITHD*) is equal to the line voltage's weighted voltage harmonic distortion factor (*VWTHD*). Practical constraints prevent the switching frequency from being increased beyond a given range.

In 60° clamping, every phase remains clamped during the middle 60° duration of every half cycle, i.e. between 60° and 120° in the positive half cycle, and between 240° and 300°

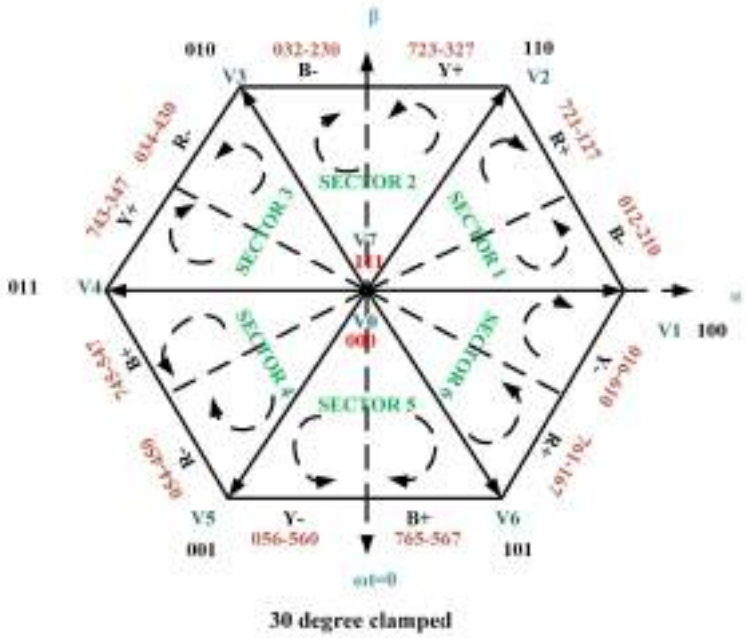

Figure 5.4. Sector Representation for a 30° Clamp SVPWM.

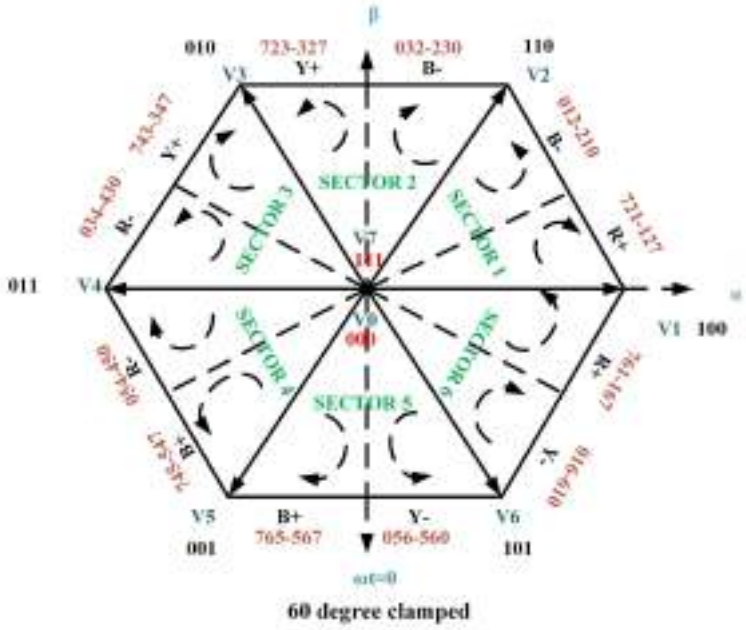

Figure 5.5. Sector Representation for a 60° Clamp SVPWM.

in the negative half cycle as shown in Figure 5.5. In type 30° clamping every phase is clamped during the middle 30° of every quarter cycle of its fundamental voltage as shown in Figure 5.4. The switching sequences for both 30° and 60° clamping are just reverse of each other and they change for every half in each sector. The switching sequences and the clamping of 30° and 60° bus clamp [9] are indicated in the figure 5.6.

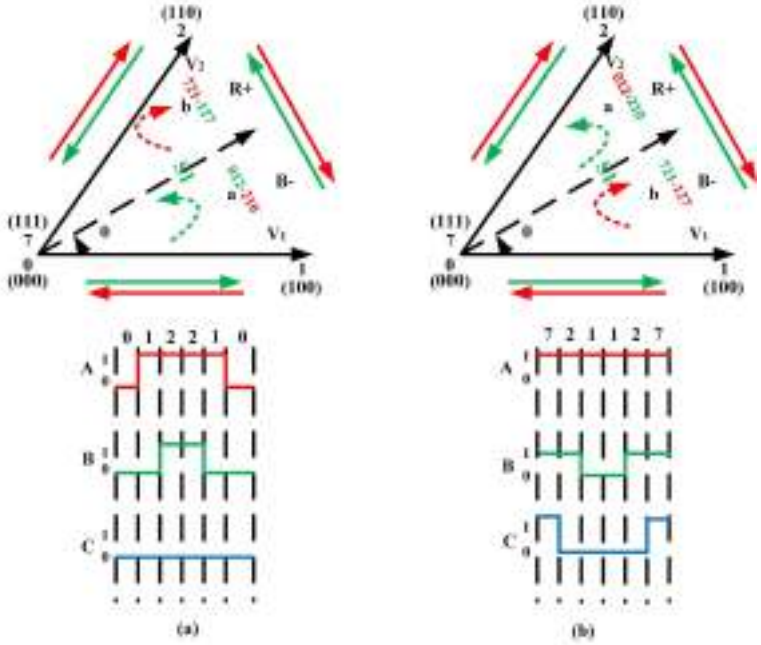

Figure 5.6. Switching Sequence for a 30° and 60° Clamp PWM.

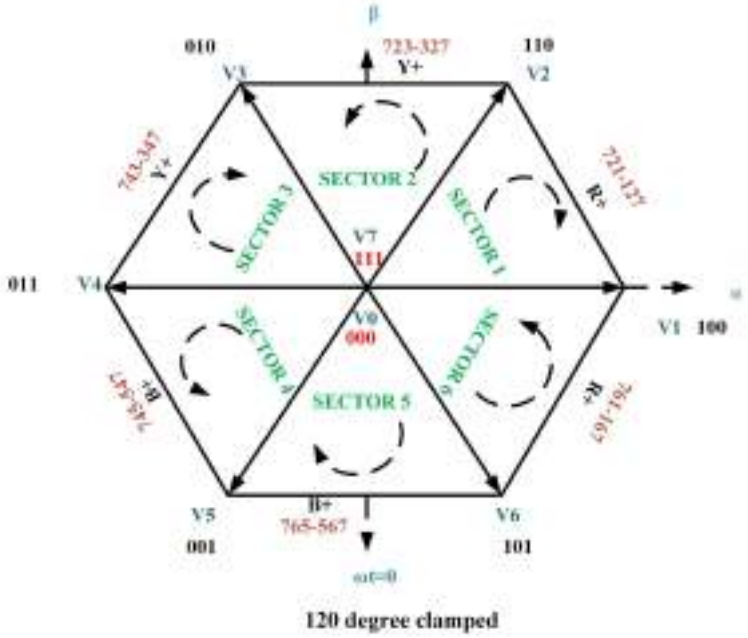

Figure 5.7. Sector Representation for a 120° Clamp SVPWM.

In the space vector technique, given a sample of the reference vector of magnitude V_{REF} and angle in sector I as illustrated in Figure 5.3, the durations for which the different vectors must be applied are determined by using voltage balance principle [7].

$$T_1 = V_{REF} \cdot \frac{sin(60 - \alpha)}{sin60} \cdot T_s \tag{5.3.1}$$

$$T_2 = V_{REF} \cdot \frac{sin(\alpha)}{sin60} \cdot T_s \tag{5.3.2}$$

$$T_z = T_s - T_1 - T_2 \tag{5.3.3}$$

here T_1 and T_2 are durations of application of active vectors V_1 and V_2 respectively. T_z is the duration of the application of zero vector. In traditional space vector modulation, the duration T_z is evenly divided between the two zero states and both are used. For a sample in sector I, either 0127 or 7210 is used. With this sequence, each phase swaps once per sub-cycle. Such sequences are known as conventional sequences.

In the 120° clamp [12], if the zero state (0) is avoided, the R-phase remains connected to the positive bus, as shown in Figure 5.7. If the zero state +++ (7) is avoided, the B-phase will remain clamped to the negative bus. Bus-clamped PWM approaches create samples using clamping sequences that have only one zero state. The zero states are modified in the center of the sector under 30° and 60° clamp designs. The zero state utilized between the center of sector VI and that of sector I is +++ (7) at 30 ° and - - - (0) at 60°.

5.4 Parameters Affected by Various BC Techniques

5.4.1 Weighted THD

The weighted voltage total harmonic distortion V_{WTHD} is calculated using the RMS values of the fundamental and n^{th} harmonic voltages in the line voltage waveform, V_1 and V_n, respectively. The weighted voltage THD is roughly proportional to the current THD and unaffected by the motor settings. The formula to calculate the V_{WTHD} [10] is given as:

$$V_{\text{wthd}} = \frac{1}{V_1}\sqrt{\sum_{n\pm1}\left(\frac{V_n}{n}\right)^2} \tag{5.4.1}$$

5.4.2 Switching Loss (P_s)

The switching loss is proportional to the DC bus voltage, the number of switches per phase, the switching sequence employed and the current passing through the device. As a result, the switching loss per sub-cycle is determined by the number of switches and the phase current.

$$P_s = 0.5 \cdot V_{dc} \cdot f_s \cdot (t_{on} + t_{off}) \cdot (n_R \cdot i_R + n_Y \cdot i_Y + n_B \cdot i_B) \tag{5.4.2}$$

where n_R, n_Y, and n_B denote the number of switches in the R, Y, and B phases, respectively. The instantaneous phase currents are denoted by i_R, i_Y, and i_B, while f_s is the switching frequency and t_{on} and t_{off} are the switch turn on and turn off times respectively.

5.4.3 Switching Frequency(f_s)

The most obvious advantage of adopting bus-clamped PWM schemes is reduced switching frequency for a given carrier frequency or sampling frequency [9]. As illustrated in Figure 5.6, each phase is clamped for 120° during each fundamental cycle. At high switching frequencies, any such approach reduces the average switching frequency to two-thirds of the carrier frequency. This indicates about a 33% reduction in switching losses. Thus, for a given carrier frequency or sampling frequency bus-clamped approaches result in a large reduction in switching frequency and losses. However, this gain comes with an increase in distortion over conventional approaches.

5.5 240° Clamped CPWM

Figure 5.8 depicts the EV power train architecture which includes a DC-DC converter that connects a relatively low-voltage battery to the inverter and high-voltage motor. This cascaded topology in EV drive trains permits greater DC-link voltages, therefore the motor speed has increased from 6000 to 17,000 r/min throughout the years, lowering the size of the motor and inverter and increasing power density. Commercial EVs, particularly hybrid EVs (HEVs) have evolved a mature architecture to interface the battery and inverter DC bus via a bidirectional DC-DC converter. The system's existing DC-DC converter makes it ideal for implementing 240°-clamped space vector PWM [13].
The dc-link voltage at the output of the dc-dc stage is dynamically regulated in both amplitude and wave shape with motor speed. The DC-AC stage is a three-phase voltage source inverter (VSI) that is switched appropriately to provide variable magnitude and variable frequency sinusoidal output voltages. The control is accomplished using several PWM approaches reported in the literature. The THD in-line current, switching losses and common mode voltage(CMV) are all affected by the exact PWM approach utilized. Figure 2 depicts a two-level, three-phase VSI with eight switching states. The reference voltage vector V_{REF} is sampled once for each subcycle, T_s. Typically, for V_{REF} with angle α in Sector I, active vectors V_1, V_2 and V_0 vectors are applied for durations T_1, T_2 and T_z respectively. Conventional space vector PWM (CSVPWM) distributes T_z equally across

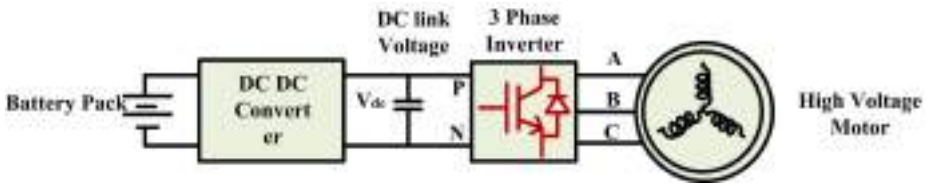

Figure 5.8. EV Powertrain architecture .

both zero states (0 and 7). It uses the 0127 or 7210 switching sequence in a subcycle in

Sector I. Three switchings occur in a subcycle with both zero states applied. The discontinuous PWM (DPWM) approaches use just one zero state, which results in two switchings every subcycle. The clamping has a great effect on the magnitude and frequency of common mode voltage. An accepted CMV metric in a star-connected three-phase electric machine is defined as the voltage between the loadstar point and the center of the dc bus, which is given by $(V_{ao} + V_{bo} + V_{co})/3$, where V_{ao}, V_{bo}, and V_{co} are the three-phase pole voltages of the inverter with respect to the dc bus center point. The usage of zero vectors results in maximum CMV values of $V_{dc/2}$ or -$V_{dc/2}$, which correspond to vectors 7 and 0, respectively. If the zero vectors are eliminated, the peak CMV can be decreased to $V_{dc/6}$. The 240° CPWM method removes zero states while requiring the fewest switchings of any PWM method, producing desired unipolar voltage waveforms, and having one of the lowest THD (high-frequency ripple) in line currents.

5.5.1 240° Concept

To synthesize a sinusoidal output voltage with a DC-AC inverter, either control the modulating signal to be sinusoidal when the dc-link voltage is fixed or control the dc-link voltage to be sinusoidal while keeping the modulating signal constant. When the dc-link voltage is dynamically regulated to produce a (piece-wise) sinusoidal waveform, the modulating signal can be clamped at appropriate intervals to connect the dc-side sine wave to the line-to-line output. 240°CPWM is a space vector modulation method that allows for the simultaneous clamping of two-phase poles. The phase poles are clamped to positive or negative DC rails for a total of 240° encompassing four sectors and switched only for 120° during each fundamental cycle as shown in figure 5.9. To synthesize the appropriate reference vector in any sector, just the two active vectors are used. Phase A is clamped to the positive DC rail in Sectors I and VI, clamped to the negative DC rail in Sectors III and IV, and switches only in Sectors II and V, according to the applied sequence of 12 in Sector I, 23 in Sector II, 34 in Sector III, and so on. Phase A is clamped for 240° as it is fixed to either positive or negative DC rail in four sectors of a basic cycle. Similarly, phases B and C are clamped for 240° and switched for 120° in a line cycle. The number of switchings for CSVPWM in a switching cycle is two per phase or six for all three stages. For 120°, phases A and B have two switches for each. However, clamping phase C results in four switching operations rather than six. The switching sequences 12–21 for 240CPWM are presented. As can be seen, phase A is clamped to the positive DC rail, phase C to the negative DC rail and switching phase B results in only two switching actions. The reference voltage vector.V_1 and V_2 are applied voltage vectors with time-varying magnitude. V_1 and V_2 represent error voltage vectors in a cycle. As a result, 240 CPWM uses the fewest amount of switches possible [14].

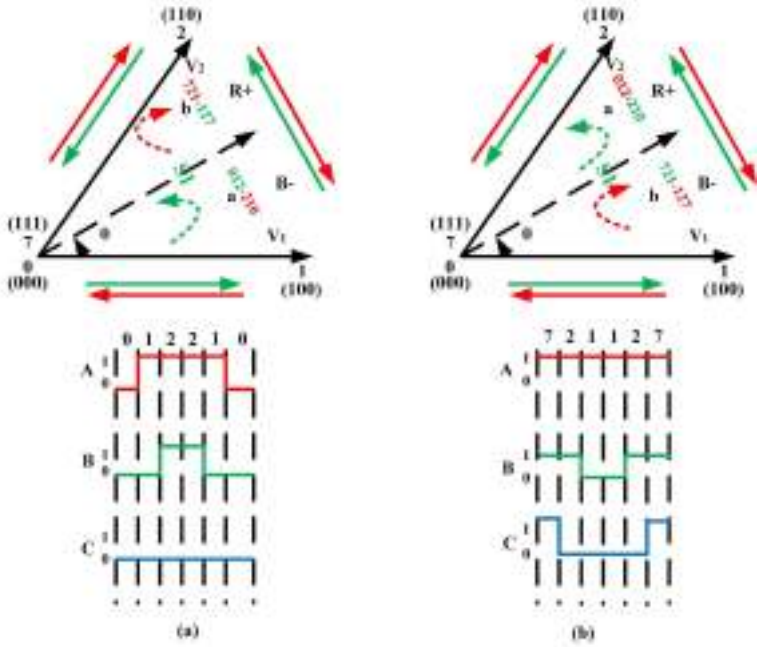

Figure 5.9. Switching Sequence for a 120° and 240° Clamp PWM.

5.6 Simulations and Results

5.6.1 CSVPWM

Figure 5.10 indicates the phase 'A' pulses generated using the space vector PWM technique. The sine wave is represented to show the alignment of pulses in all the clamping techniques. In CSVPWM the currents produced at the output terminals are more sinusoidal compared to all other clamping techniques as shown in Figure 5.11. The torque profile is more smoother as shown in Figure 5.12. The CMV produced in the CSVPWM method contains all the levels producing higher peaks as shown in Figure 5.13.

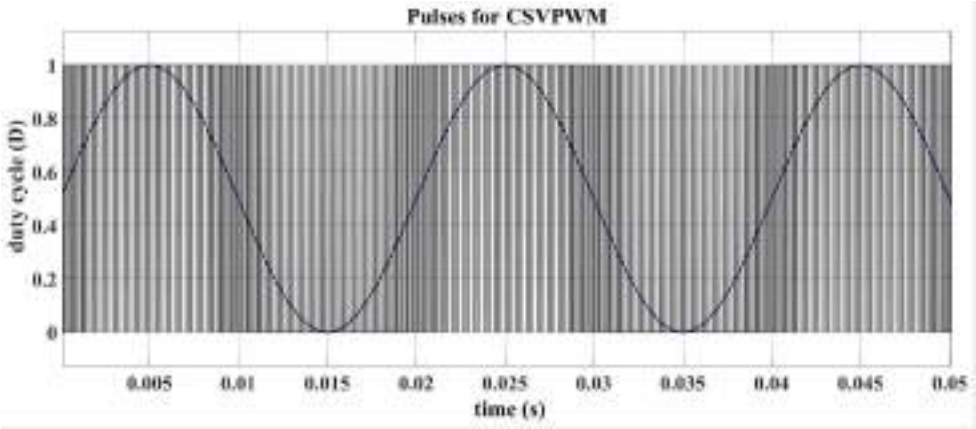

Figure 5.10. Pulses in Conventional SVPWM.

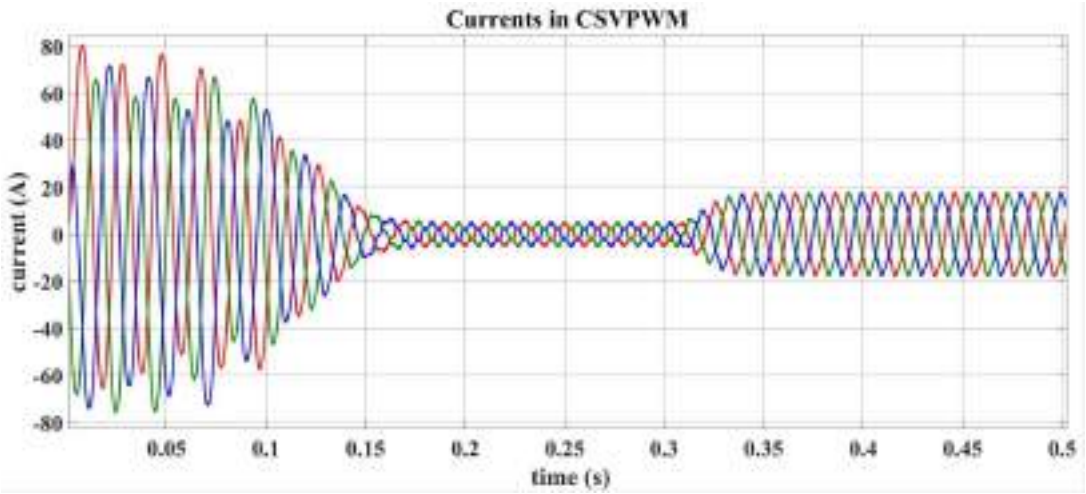

Figure 5.11. Stator currents in Conventional SVPWM.

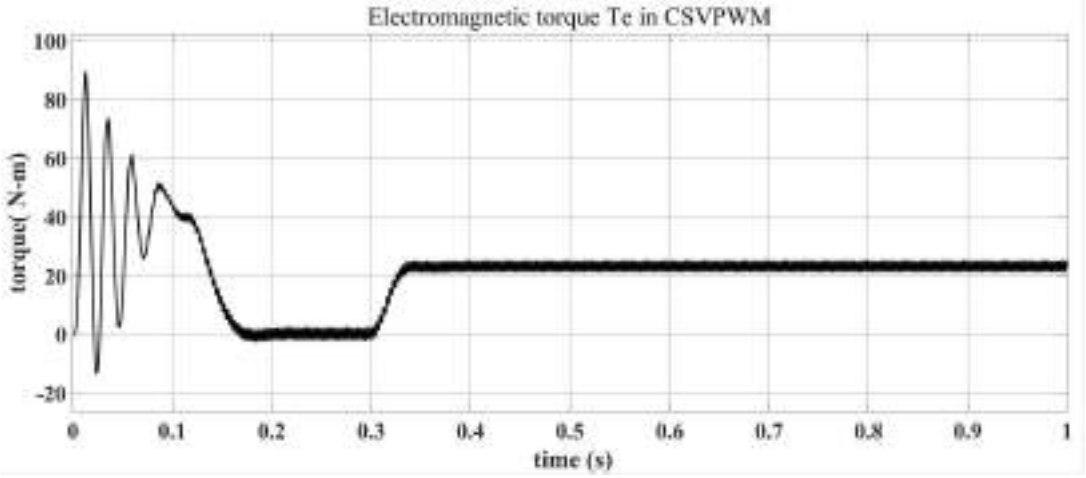

Figure 5.12. Electromagnetic Torque in Conventional SVPWM.

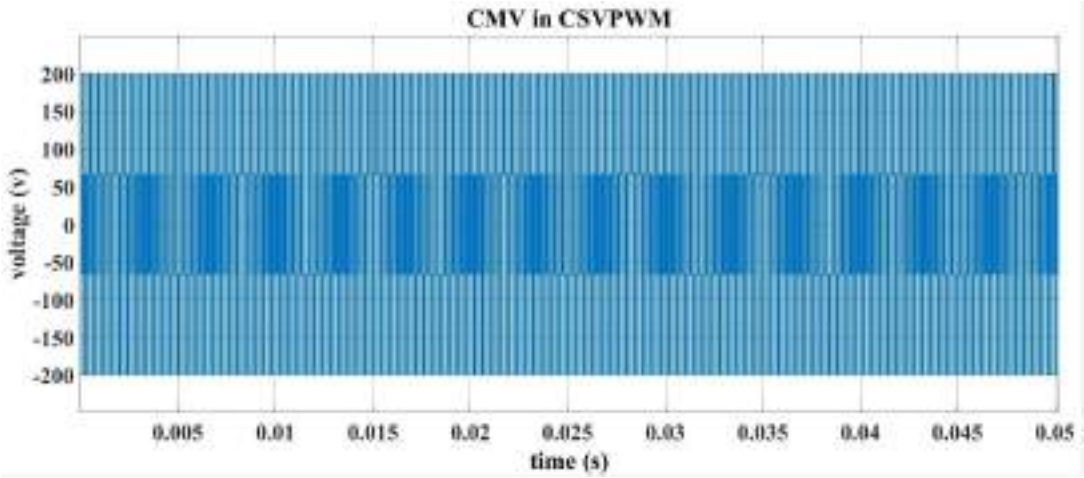

Figure 5.13. Common mode voltage in Conventional SVPWM .

5.6.2 30° Clamp SVPWM

Figure 5.14 depicts the pulses generated for phase 'A', it clamps for a total of 60° in each half cycle at quarter half cycles. The torque performance has degraded a little as shown in figure 5.15, it contains more ripples. The CMV waveform peak magnitudes are not removed but the frequency of peak magnitudes is reduced as shown in figure 5.16.

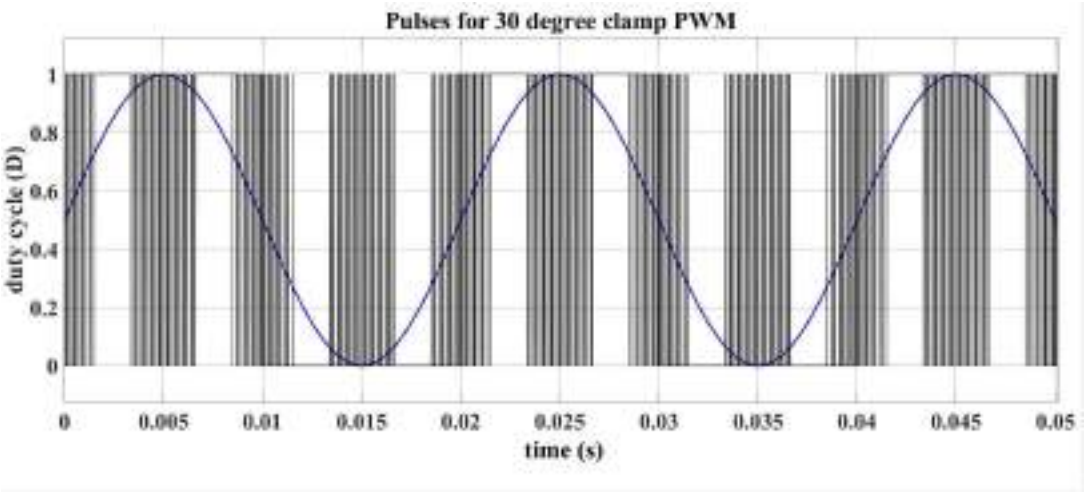

Figure 5.14. Pulses in 30° Clamp SVPWM

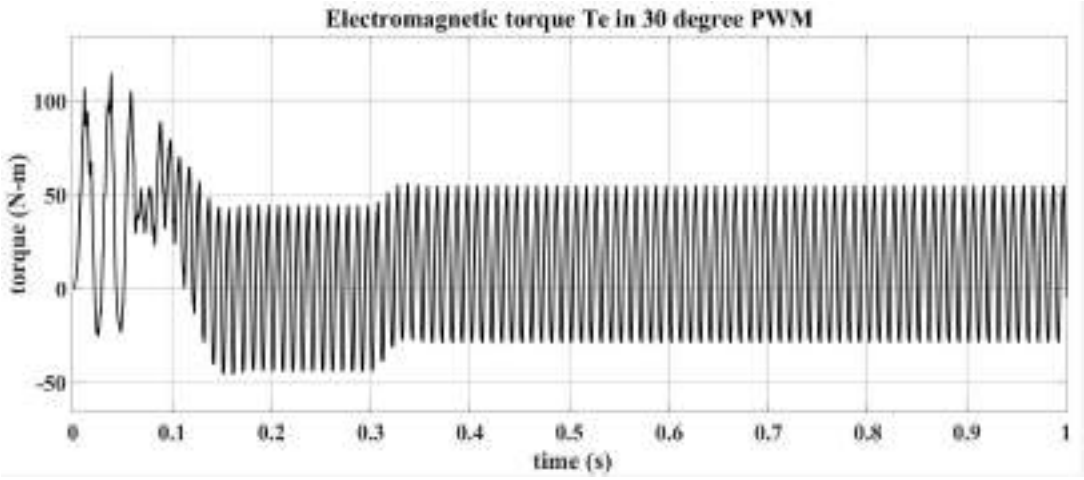

Figure 5.15. Electromagnetic Torque in 30° Clamp SVPWM .

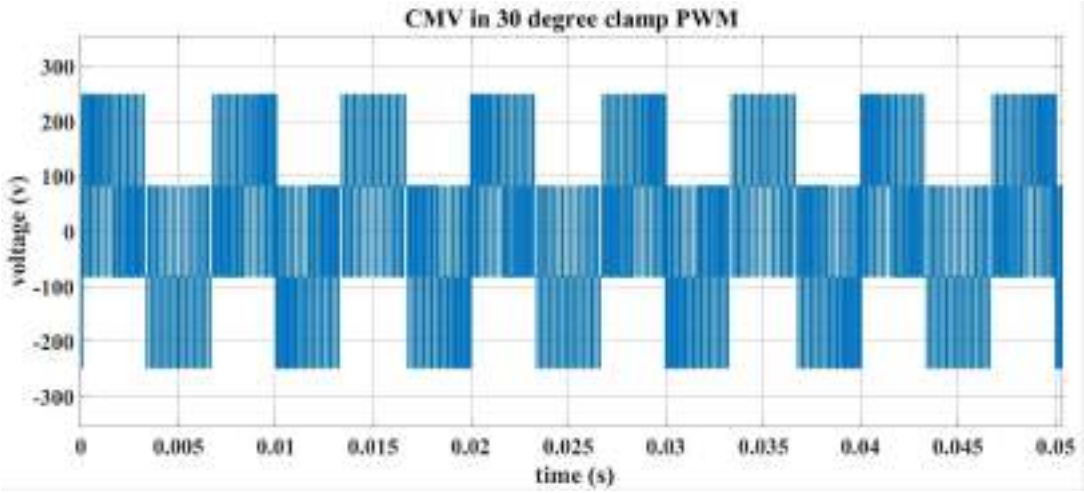

Figure 5.16. CMV in 30° Clamp SVPWM .

5.6.3 60° Clamp SVPWM

Figure 5.17 depicts the pulses generated for phase 'A', it clamps for a total of 60° in each half cycle at a time in the mid. The torque performance is a little better than 30° as shown in Figure 5.18, it contains more spikes. The CMV waveform is almost similar to 30° clamp PWM, shown in Figure 5.19.

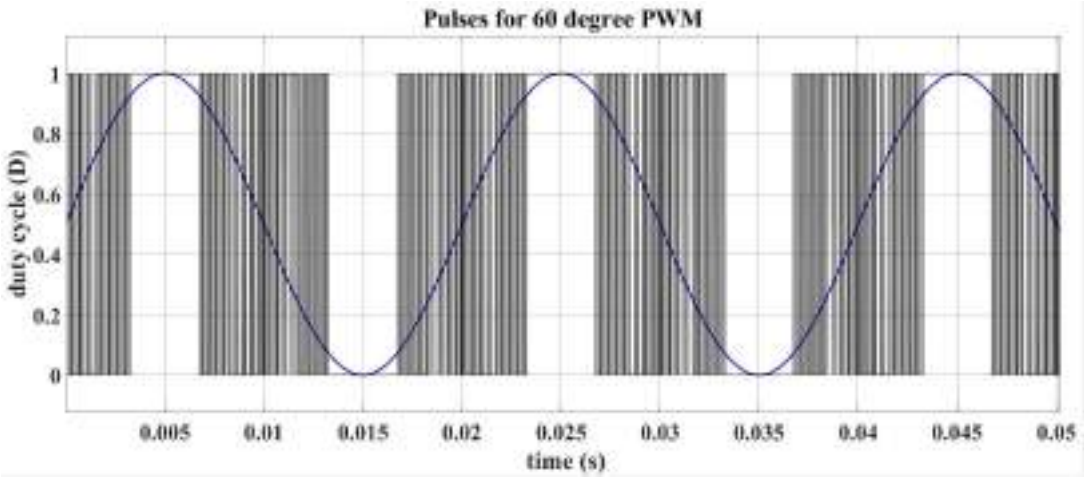

Figure 5.17. Pulse Generation in 60° Clamp SVPWM .

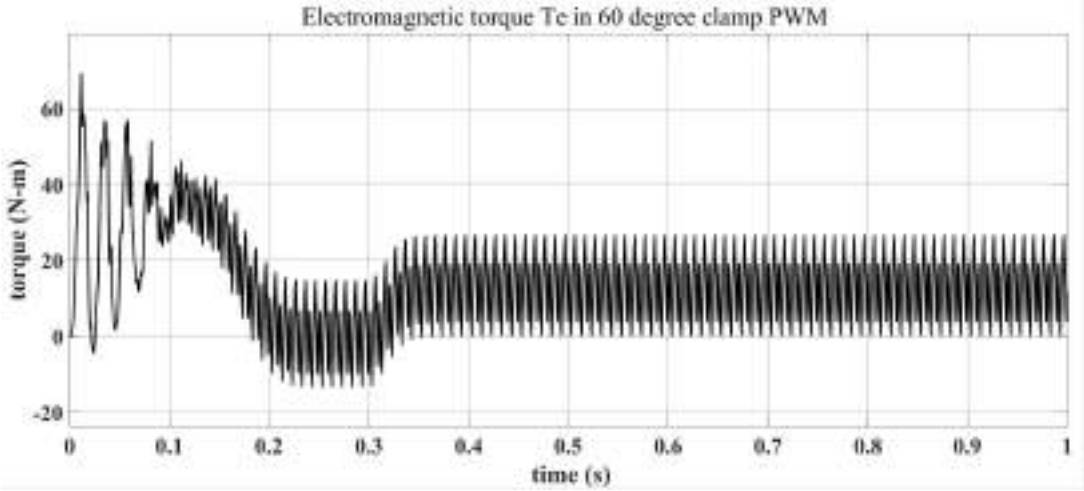

Figure 5.18. Electromagnetic Torque in 60° Clamp SVPWM.

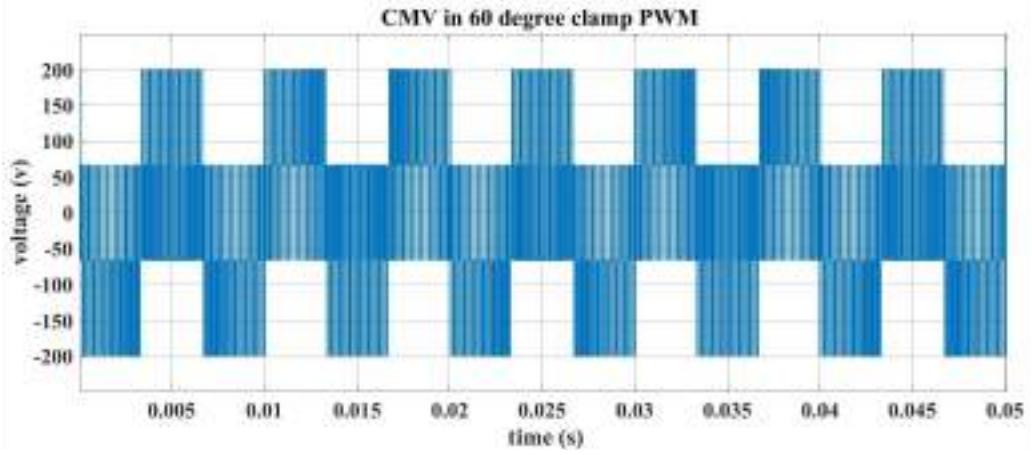

Figure 5.19. Common mode voltage in 60° Clamp SVPWM.

5.6.4 120° Clamp SVPWM

Pulse generation for the 'A' phase in 120° clamp SVPWM is shown in Figure 5.20, since only one zero state is used (+++) the clamping of 120° is towards the positive dc bus. The torque response is shown in Figure 5.21, which is better than other bus clamp methods. The CMV levels are reduced and the negative peak is removed as shown in figure 5.22.

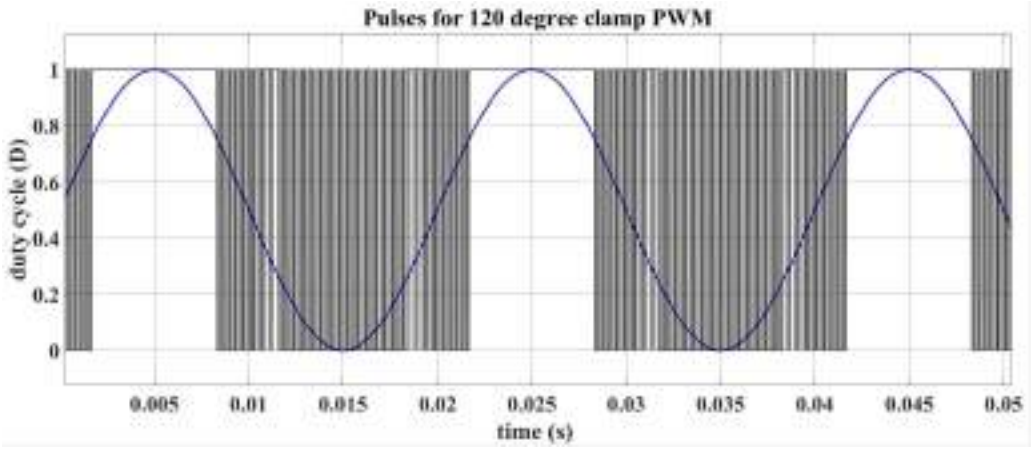

Figure 5.20. Pulses in 120° Clamp SVPWM .

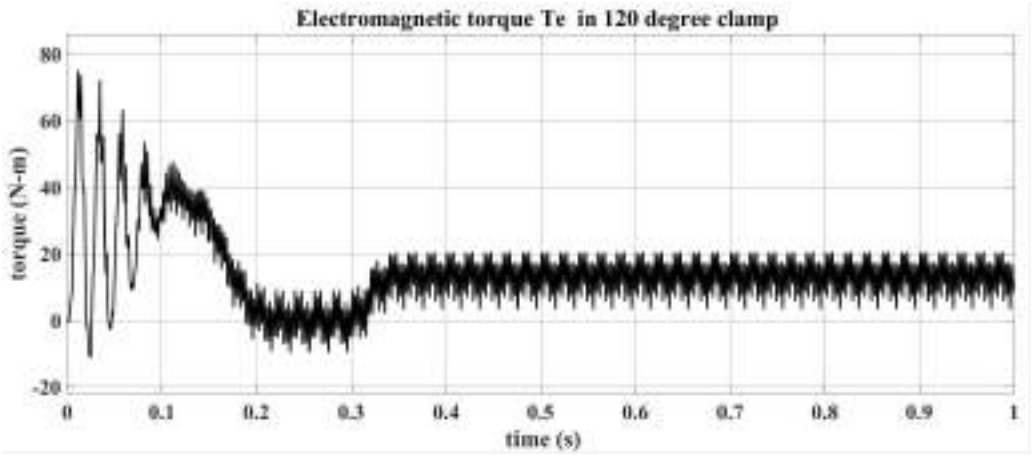

Figure 5.21. Electromagnetic Torque in 120° Clamp SVPWM .

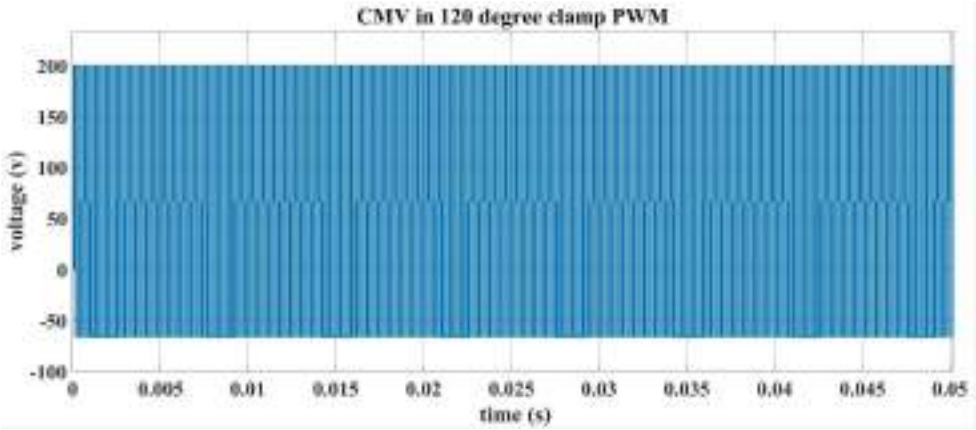

Figure 5.22. Common mode voltage in 120° Clamp SVPWM.

5.6.5 240° Clamp SVPWM

Figure 5.23 depicts the pulse generation of the 'A' phase, producing each 120° clamp in positive and negative half cycles. The currents are smoother compared to other clamping techniques as shown in Figure 5.24. The torque response is smoother, reducing the ripple content and the spikes as shown in Figure 5.25. Finally, only 2 levels of common mode voltage are produced as shown in Figure 5.26. The high magnitude and high frequency of CMV are reduced finally.

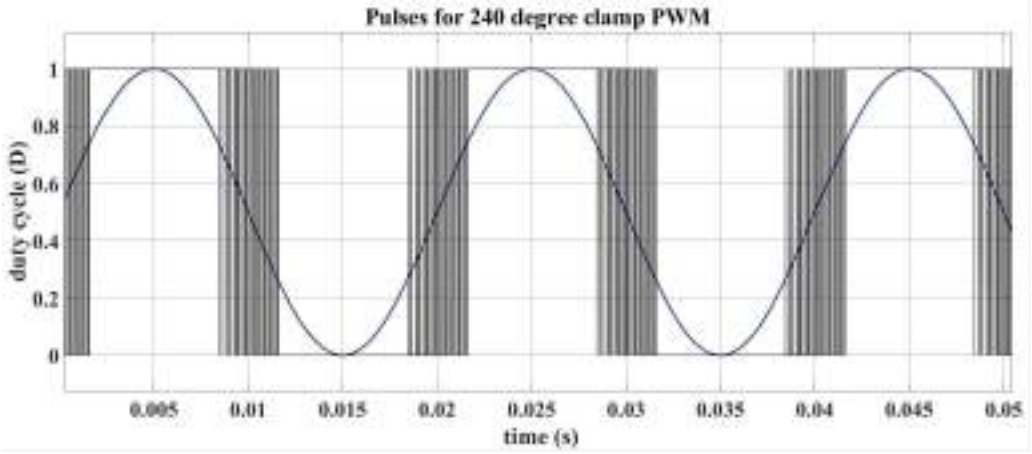

Figure 5.23. Pulses in 240° Clamp SVPWM .

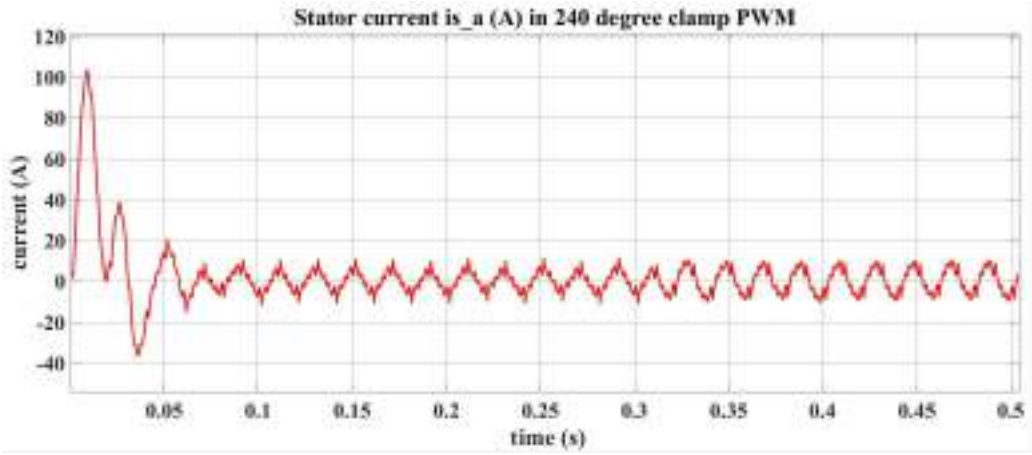

Figure 5.24. 'A' Phase Stator Current in 240° Clamp SVPWM .

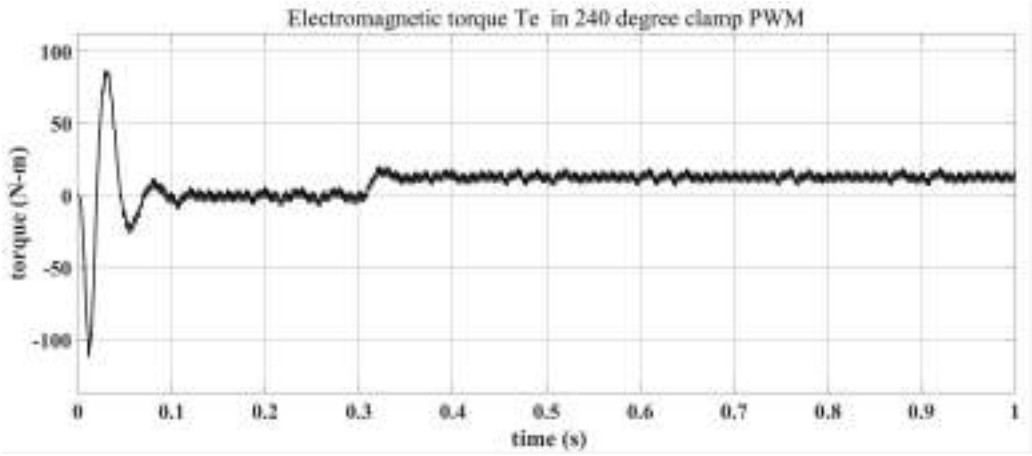

Figure 5.25. Electromagnetic Torque in 240° Clamp SVPWM .

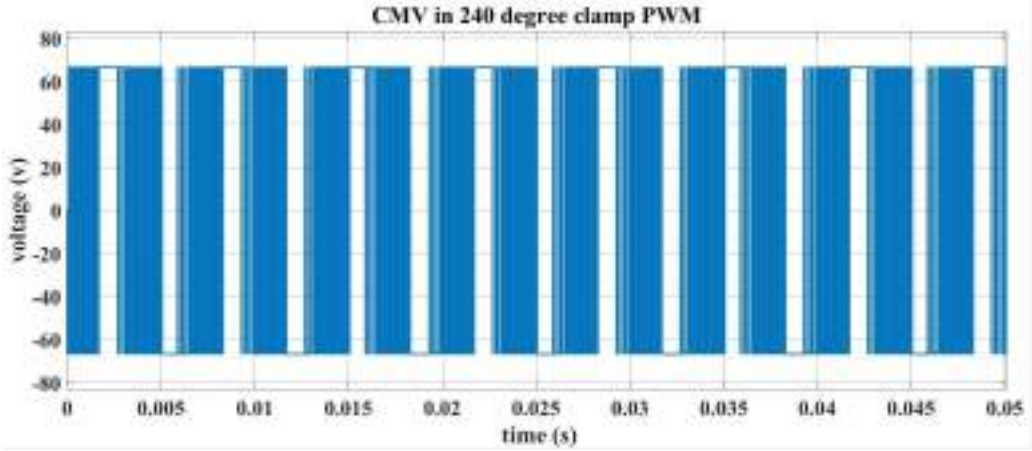

Figure 5.26. Common mode voltage in 240° Clamp SVPWM .

Table 5.2: No of Switchings in Three-Phase

Parameter	**CSVPWM**	**30° CLAMP**	**60° CLAMP**	**120° CLAMP**	**240° CLAMP**
No of switchings	6	4	4	4	2

Table 5.3: THD Comparison Values with Varying Modulation Indices

Modulation index(m)	**Parameters**	**CSVPWM**	**30° Clamp**	**60° Clamp**	**120° clamp**
m=0.7	Current THD(%)	5	29.22	67.62	85.08
	Fundamental Current (A)	14.1	13.84	13.3	10.77
	Voltage THD(%)	51.4	82.32	95.91	117.59
	Fundamental Voltage(V)	290.8	272.6	230	259.1
m=0.8	Current THD(%)	4.58	25.13	48.67	73
	Fundamental Current (A)	16.1	18.6	15.28	9.6
	Voltage THD(%)	49.4	66.9	89.59	113.10
	Fundamental Voltage(V)	305	318.2	264.5	364.9

5.7 Conclusion

Different bus clamping techniques have been performed on a three-phase two-level inverter fed induction motor and various performance parameters like THD, CMV, torque ripples and number of switching are compared . Out of all the techniques 240 degree clamp produces less number of switchings as shown in table 5.2. It produces lesser CMV, reducing both in magnitude,frequency and also produces better torque performance.

Chapter 6

CMV REDUCING TECHNIQUES IN MULTILEVEL INVERTERS

6.1 Introduction to Multilevel Inverters

ML-VSIs are increasingly used in LV and MV commercial, industrial and utility applications due to their ability to handle high voltage levels and produce the minimum THD output without requiring costly advancements, filters, or transformers and the need for PWM can be avoided entirely [15]. The ML VSI synthesizes the AC output voltage by connecting capacitor voltage dividers or DC power supply in series and uses high-speed switches. As the number of levels increases, the ML-VSI's output voltage takes on a staircase appearance. As the number of levels approaches infinity, the output voltage becomes sinusoidal and the output THD decreases to zero. Producing multi-layer waveforms is a commonly utilized method. Multilevel waveforms are commonly utilized to minimize harmonic content while maintaining output power. There are numerous advantages of ML-VSIs over two-level VSIs. PWM operation reduces current ripple for the same switching frequency, allowing for lower switching frequencies while maintaining the same current quality. This reduces the inverter's overall switching losses. ML-VSIs can sustain larger voltages than two-level VSIs, providing an additional advantage. In a two-level VSI, each switching device must block the DC bus voltage. Device stress scales inversely with the number of levels in ML-VSIs, starting with three levels. Therefore, with increasing the number of levels, the voltage stress on switching devices reduces which results in higher rated output power and voltage. The main trade-off is ML-VSIs result in a significant rise in switching devices as the number of levels increases. On a case-by-case basis, calculate the minimal number of levels needed to meet system criteria such as voltage rating, output power, minimum THD, fault tolerance, and dependability.

In terms of CMV, ML-VSIs outperform two-level inverters significantly. The CMV in ML-VSIs has lower dv/dt due to its higher voltage steps across the DC bus voltage range. ML-VSIs experience less DM overvoltage transients at motor terminals when lengthy ca-

bles are used. Distributed impedance on lengthy motor cables can result in peak transient voltage up to 2 times the DC bus voltage, assuming full decay of prior pulses. Using a three-level inverter would result in transient peaks of only 1.5 pu of the DC bus voltage.

6.2 Classification of Multi-level Inverters

An ML-VSI inverter generates three or more levels of output pole voltage. This involves adding more semiconductor switches, DC power supplies, capacitors and diodes. This section will explain the three primary classes of ML-VSIs. MLIs are classified into three types [16]:

1. Diode-Clamped (NPC)
2. Flying Capacitor (FC)
3. Cascaded H-Bridge (CH).

6.2.1 Neutral Point Clamped Converter NPC)

The ML NPC VSI, like the two-level VSI, connects each output phase to the middle of each inverter pole's switches. Each switch has a freewheeling diode and each phase requires clamping diodes. Assuming m is the number of levels, the number of active switching devices per phase is 2(m-1). A series of (m-1) capacitors can produce 'm' levels of output voltage by dividing voltage. Under balanced conditions, the voltage across each capacitor equals $V_{dc}/(m-1)$, which corresponds to the voltage required to block each active switch. In ML-NPC VSI the special advantage is as the number of levels increases, the blocking voltage decreases.

As the number of levels increases, the clamping diodes block more capacitor voltage levels. VSIs require a quadratic number of diodes (m-1)(m-2) for each phase to maintain the voltage rating of each diode. Using a standard PWM algorithm at rated conditions results in a line-to-line voltage of (2m-1) at the NPC VSI output. If the inverter output is driving a Y-connected load, then the phase voltage will take on (4m-3) levels [17].

There are various pros and cons to NPC MLIs. Adding clamping diodes to the NPC structure boosts the system's KVA rating by increasing the DC bus voltage while minimizing switching device voltage stress. This sort of inverter allows for reactive power transfer without altering the capacitor voltage balance. However, active power control, such as grid-linked applications, is challenging to achieve. If the NPC inverter is constructed for worst-case scenarios, the 2(m-2) outer switches will be oversized due to the longer switch-on times required by the inner switches, especially at low switching frequencies and modulation index. If designed for typical service, inner switches may be undersized.

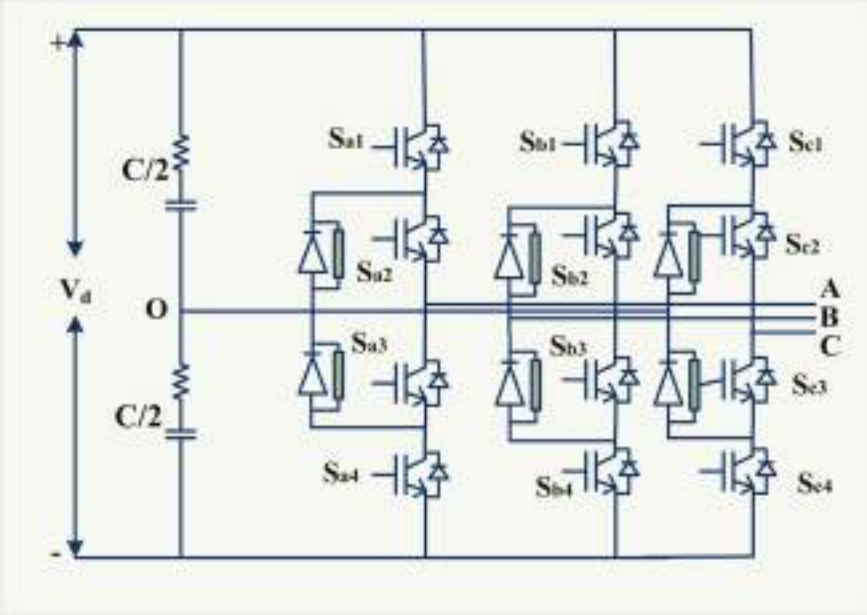

Figure 6.1. Three-Phase 3 level NPC Converter

The capacitors require pre-charge circuitry to limit the capacitor current when energizing the DC bus. The NPC MLI's ability to pre-charge capacitors as a group makes it easier to execute this function compared to other MLI models. The NPC MLI's three phases rely on the same capacitor bank which can be problematic if the DC bus fails. The ML-VSI has the advantage of reducing CMV step height as inverter levels grow. Using a CMV mitigation PWM approach in an NPC MLI may affect capacitor voltage balancing by not utilizing redundant switching states.

6.2.2 Working of a three-Level NPC

A three-phase three-level NPC consists of 4 switches per leg and in total 12 switches for a three-phase configuration. It contains 2 diodes per phase and in total of 6 clamping diodes for three phases. The diodes clamp the midpoint voltage, resulting in equal voltage distribution among the four IGBTs within each phase leg. Three-level VSCs can generate three voltage levels $\frac{V_{dc}}{2}$, 0 and -$\frac{V_{dc}}{2}$ per phase between 'A' and 'O'.The DC link is equally divided by (N-1) capacitors where N is no of levels [17]. In Table 6.1, x= a, b, c denotes the three-phase assignment. Each inverter pole consists of four series-connected IGBTs generalized as S_{x1}, S_{x2}, S_{x3}, S_{x4} with accompanying anti-parallel diodes linked across the dc bus, as well as two clamping diodes D_{x1} and D_{x2} with their common point connected to the dc bus's midway point 'O'. If S_{x1} and S_{x2} are on, D_{x2} (clamping diodes) balances the voltage across S_{x3} and S_{x4}. As a result, S_{x3} blocks the voltage across C_1, while S_{x4} blocks

the voltage across C_2. A similar operation can be observed when S_{x2} and S_{x3} are turned on, as well as S_{x3} and S_{x4} . The applied voltage collectively shared by the two capacitors is $\frac{V_{dc}}{2}$. Similar to the two-level VSI, each inverter leg's output connects to the midpoint of the IGBTs, which can switch between three states. When IGBTs S_{x1} and S_{x2} are turned on, the output is connected to the positive dc bus $\frac{V_{dc}}{2}$, when IGBTs S_{x3} and S_{x4} are turned on, the output is connected to the negative dc bus -$\frac{V_{dc}}{2}$. The third output state is obtained when S_{x2} and S_{x3} are on and hence the output gets connected to the midpoint of the dc bus producing 0 levels by D_{x1} for positive output current as shown in figure 6.2 and D_{x2} for negative output current as shown in figure 6.3.

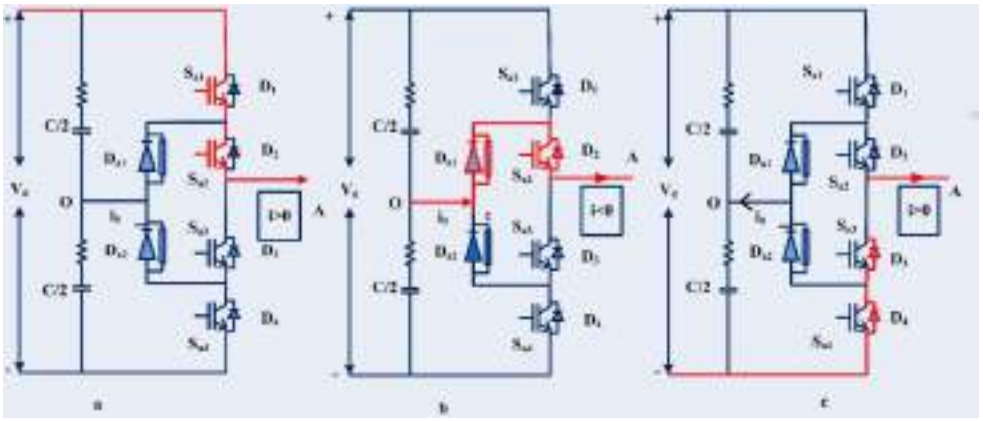

Figure 6.2. Current Flow During Positive Half Cycle

	V_{AO}	S_{a1}	D_1	S_{a2}	D_2	S_{a3}	D_3	S_{a4}	D_4	D_{a1}	D_{a2}	
i>0	$\frac{V_{dc}}{2}$	on		on								a
	0			on						on		b
	-$\frac{V_{dc}}{2}$						on		on			c

Table 6.1: Working Switches During Positive Half Cycle

	V_{AO}	S_{a1}	D_1	S_{a2}	D_2	S_{a3}	D_3	S_{a4}	D_4	D_{a1}	D_{a2}	
i<0	$\frac{V_{dc}}{2}$		on		on							a
	0					on					on	b
	-$\frac{V_{dc}}{2}$					on		on				c

Table 6.2: Working Switches During Negative Half Cycle

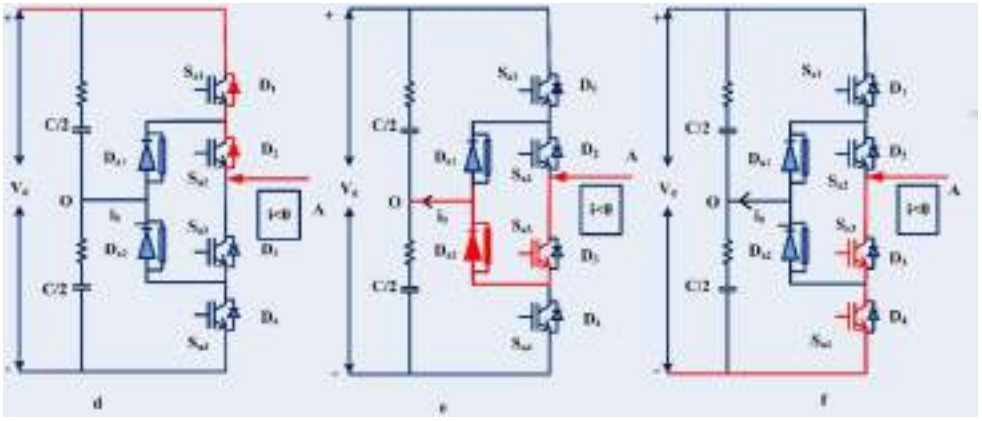

Figure 6.3. Current Flow During Negative Half Cycle

6.3 Techniques to Reduce CMV in Three-Level NPC

Controlling a three-level VSI with PWM is the most popular technique. It is commonly employed in motor-drive systems because of its several benefits over traditional commutation methods. To reduce losses and torque Pulsations the harmonic content in the output should be minimized. Three-level PWM schemes have been integrated into three-level ASDs, replacing the traditional 12-step commutation mode, which has poor harmonic performance due to square-wave output voltages. Various types of PWM can be used in three-level VSIs, including open-loop feedforward schemes like SPWM, SV-PWM, SHE-PWM, D-SPWM, and closed-loop feedback systems like predictive current control. ASDs typically use PWM approaches to achieve certain aims. Other objectives, such as eliminating harmonics or reducing inverter output voltage THD, may also be achieved. PWM strategies can also be devised to minimize switching losses.

6.4 Double Modulating Reference Wave Techniques

The NPC three-level inverter with conventional modulation requires 50% more dc-link capacitance than a two-level inverter for fixed grid frequency operation. Electrolytic capacitors are necessary for high capacitance values [18]. In the neutral point clamped converters, using the CBPWM approach, the neutral point current has a frequency three times higher than the output fundamental frequency. Thus, it requires a huge DC-link capacitor to remove the neutral point oscillations. Small dc-link capacitors in drives provide low input line current total harmonic distortion THD compared to massive dc-link capacitors. To avoid output voltage, current distortion as well as switch over-voltage, the low-frequency voltage oscillation button at the neutral position should be removed. Small film capacitors are preferred as DC-link capacitors for a dependable and cost-effective system. Various technologies have been explored in this regard. Control strategies like CBPWM

or SVPWM approaches can eliminate the low-frequency component of the neutral point current under certain operating situations, but not all. Low-frequency oscillations continue to exist at neutral points. These tend to unbalance the capacitor voltages. Large DC-link capacitors are required to reduce oscillations under specific operating conditions. Many solutions have been proposed to eliminate the neutral point oscillations which is the major issue in NPC. But as it is known, the reduction of CMV is also important because high CMV may cause some unwanted drawbacks such as producing over-voltage stress to the winding insulation, increasing EMI, resulting in high-frequency overload bearing current, etc. NPC inverters feature several switching states that can eliminate or reduce CMVs. This trait has led to numerous software solutions for CMV mitigation. Using different vectors, the CMV can be reduced to only one-sixth of the dc-link voltage and this is already shown using BUS clamping methods in the previous chapter for a 2-level inverter. To have further flexibility in the reduction of CMV, multi-level topologies are preferred. Adopting the method of double modulating wave and its reversal technique can further help to eliminate the neutral point oscillations along with the reduction of common mode voltage in NPC's. By reducing the neutral point oscillations the size of the DC link capacitors can be reduced which further helps in saving the cost [20]. Modifying reference signals can assure a zero average neutral-point current during switching under ideal conditions, such as a high inductive load and optimal switching devices. Neutral-point voltage can vary due to component non-idealities, transients, and other factors. This chapter's first half proposes a compromise solution for CMV reduction along with the neutral point oscillation elimination using double wave CBPWM strategy. The two main contributions are :

1. A general double wave CBPWM approach that eliminates neutral point voltage low-frequency oscillations is strictly derived.

2. A strategy for reducing CMV based on double wave CBPWM

To produce a zero average neutral point current using SPWM, add common mode offsets to the reference signals and ensure the middle voltage phase has four transitions during the switching period. The modulation waves U_{ma}, U_{mb}, and U_{mc} can be defined as

$$U_{ma} = m \cdot cos(\omega t) \tag{6.4.1}$$

$$U_{mb} = m \cdot cos(\omega t - \frac{\pi}{3}) \tag{6.4.2}$$

$$U_{mc} = m \cdot cos(\omega t + \frac{2 \cdot \pi}{3}) \tag{6.4.3}$$

The modulation index 'm', ranges from 0 to 1. If the zero sequence component is injected, m can be bigger than one. The average current from the neutral point throughout a carrier

period can be stated as [19]:

$$i_{NP} = d_{ao} \cdot i_a + d_{bo} \cdot i_b + d_{co} \cdot i_c \tag{6.4.4}$$

The zero state (connecting to o) duty cycle d_{xo} (x = a, b, c) is defined as the ratio of zero state duration in (connecting to P) duty cycle d_{xp} and the negative state (connecting to n) duty cycle d_{xn}. All duty cycles must satisfy the constraint d_{xo}+d_{xo}+d_{xo}=*1*. The general expression for d_{xo} is

$$d_{xo} = 1 - |U_{mx}| \tag{6.4.5}$$

If the power factor angle is ϕ, then the output currents can be formulated as follows:

$$i_a = I_0 \cdot \cos(\omega t - \phi) \tag{6.4.6}$$

$$i_b = I_o \cdot \cos(\omega t - \phi - \frac{2\pi}{3}) \tag{6.4.7}$$

$$i_c = I_o \cdot \cos(\omega t - \phi + \frac{2\pi}{3}) \tag{6.4.8}$$

substituting both equations in i_{NP} gives

$$i_{NP} = (1 - |U_{ma}|) \cdot i_a + (1 - |U_{mb}|) \cdot i_b + (1 - |U_{mc}|) \cdot i_c \tag{6.4.9}$$

Higher modulation index (m) and output current (I_o) result in a higher neutral point current (i_{NP}). To prevent voltage oscillation on the neutral point with small dc-link capacitors, large dc-link capacitors should be used. Otherwise, the output voltage and current will be distorted, and the switches will experience over-voltage.

6.4.1 Non-Reversed Double Modulating Wave

By using the double modulation waves CBPWM approach, each phase's output can have three states within a carrier period. This allows for a more flexible distribution of positive and negative duty cycles. Duty cycles are expressed as: From these duty cycles two modu-

Phase	d_{xp}	d_{xn}	d_{xo}
a	$\frac{U_{ma}}{2} + d_{off}$	$1 - d_{ap} - d_o$	d_o
b	$\frac{U_{mb}}{2} + d_{off}$	$1 - d_{bp} - d_o$	d_o
c	$\frac{U_{mc}}{2} + d_{off}$	$1 - d_{cp} - d_o$	d_o

Table 6.3: Duty Cycles

lating waves U_{xp} and U_{xn} (x = a,b,c) corresponding to each phase are developed as shown in figure 6.4 for 'a' phase. U_{xp} is the positive modulation wave, which produces two states

p and o, controlling switches S_{x1} and S_{x3}. U_{xn} is the negative modulation wave, which produces two states n and o controlling switches S_{x4} and S_{x2} as shown in the figure 6.5.

$$U_{xp} = d_{xp} \tag{6.4.10}$$

$$U_{xn} = 1 - d_{xn} \tag{6.4.11}$$

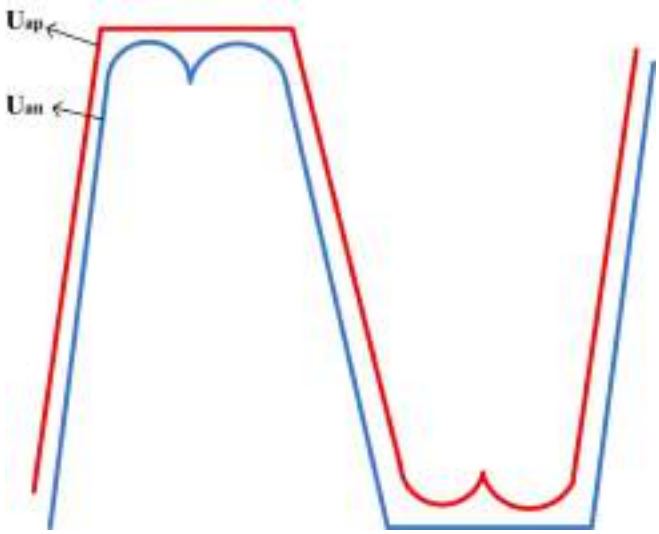

Figure 6.4. Modulating Wave Forms in Non-Reversed Double Modulating Method

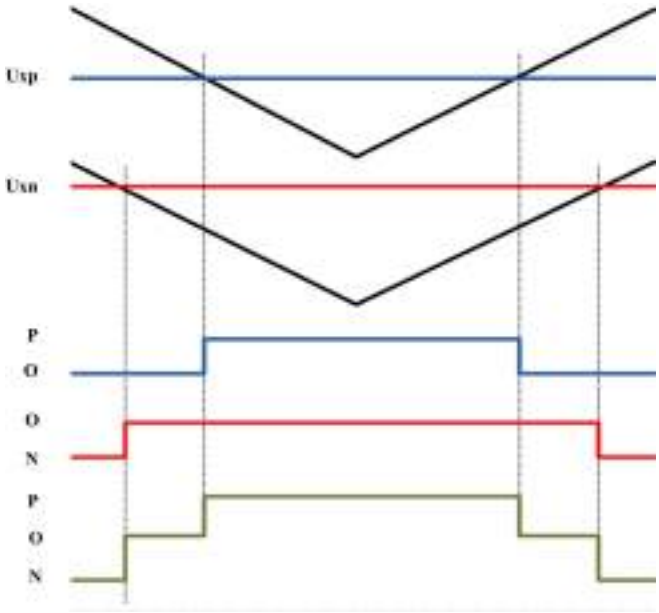

Figure 6.5. Three-Level Generation in Non-Reversed Double Modulating Method

6.4.2 Reversed Double Modulating Method to Reduce CMV

Out of 27 vectors, only 7 voltage vectors can eliminate the CMV. However, the voltage oscillation on the neutral point cannot be eliminated with these vectors alone. To lower the amplitude of the CMV, avoid employing voltage vectors such as V_o (ppp), V_o (nnn), and V_{S1} (onn), V_{S2} (ppo), V_{S3} (non), V_{S4} (opp), V_{S5} (nno), and V_{S6} (pop). This will limit the CMV to $\pm\frac{V_{dc}}{6}$. The switching sequence includes small vectors V_{S1}(onn) and V_{S2}(ppo), resulting in a CMV with amplitude $\pm\frac{V_{dc}}{3}$. To eliminate these vectors, modify the switching sequence. If the switching sequence of the phase corresponding to U_{max} is reversed, the initial state becomes p, followed by o and then$p$ as shown in figure 6.6. The modified modulating waveform equations are

$$U_{xp} = 1 - d_{xp} \tag{6.4.12}$$

$$U_{xn} = d_{xn} \tag{6.4.13}$$

The blue line represents the output state of the modulation wave U_{xp}, the red line represents

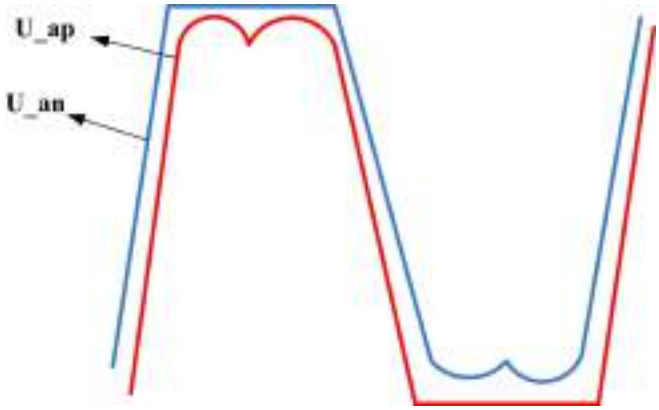

Figure 6.6. Modulating Wave Forms in Reversed Double Modulating Method

the output state of modulation wave U_{xn}, and the black line represents the combined output state as shown in figure 6.7, which is reorganized in reverse order and corresponds well to the duty cycles. Phase a's switching sequence is reversed by swapping the positive and negative modulation waveforms as shown in figure 6.6.

6.5 A CB-PWM Technique to Reduce Instantaneous CMV to Nearly Zero

The above-discussed techniques can only reduce CMV up to some maximum limit $\frac{V_{dc}}{6}$. This new CB-PWM technique makes the instantaneous CMV produced by the VSI, at all

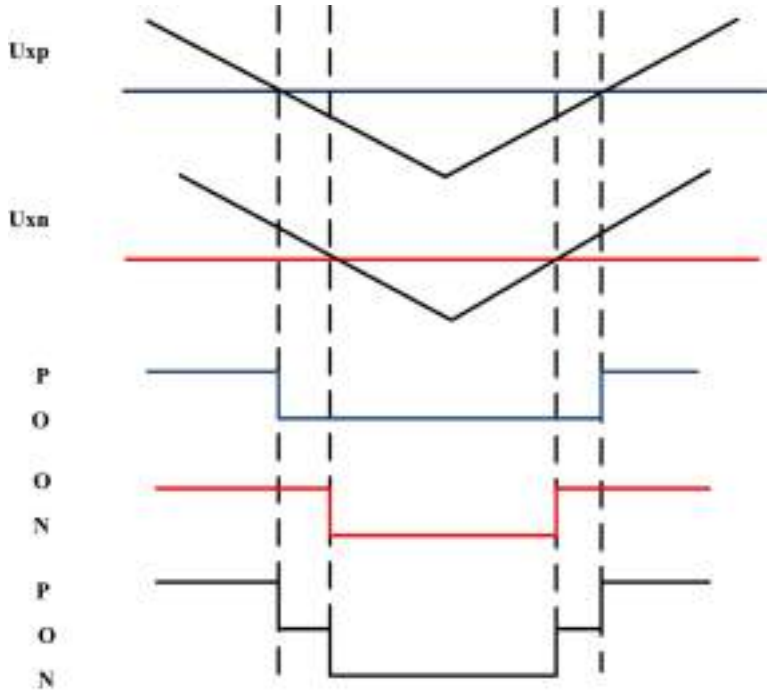

Figure 6.7. Three-Level Generation in Reversed Double Modulating Method

the instants 0 [21]. It works on the concept of a virtual level. The real x- x-level of VSI is transformed into a virtual y-level by using an algorithm depicted in the flowchart 6.8. This method requires less hardware and also can be easily extended to multi-phase systems with multi-level. As the motive was reducing CMV on a three-phase three-level NPC, the virtual transformation according to the flowchart can be transformed as follows:

$$y = \frac{(x+1)}{2} \tag{6.5.1}$$

As x= 3 in this case, the virtual level to be determined is 2.

$$y = 2 \tag{6.5.2}$$

The instantaneous pole voltage V_i^x of the ith phase of an x-level q–phase VSI can be formulated as:

$$V_i^x = \frac{V_{dc}}{2 \cdot (x-1)} \cdot S_i^x \tag{6.5.3}$$

The summation of the pole voltage of all phases divided by the number of phases gives the CMV of a VSI in terms of switching function. The CMV can be expressed as:

$$V_{cm} = \frac{1}{q} \cdot \frac{V_{dc}}{2 \cdot (x-1)} \cdot S_i^x \tag{6.5.4}$$

where 'q' is number of phases and S_i^x is an integer which varies from $(x-1)$ to $(-x+1)$ in steps of 2. The choice for the maximum phase difference between fundamental voltages

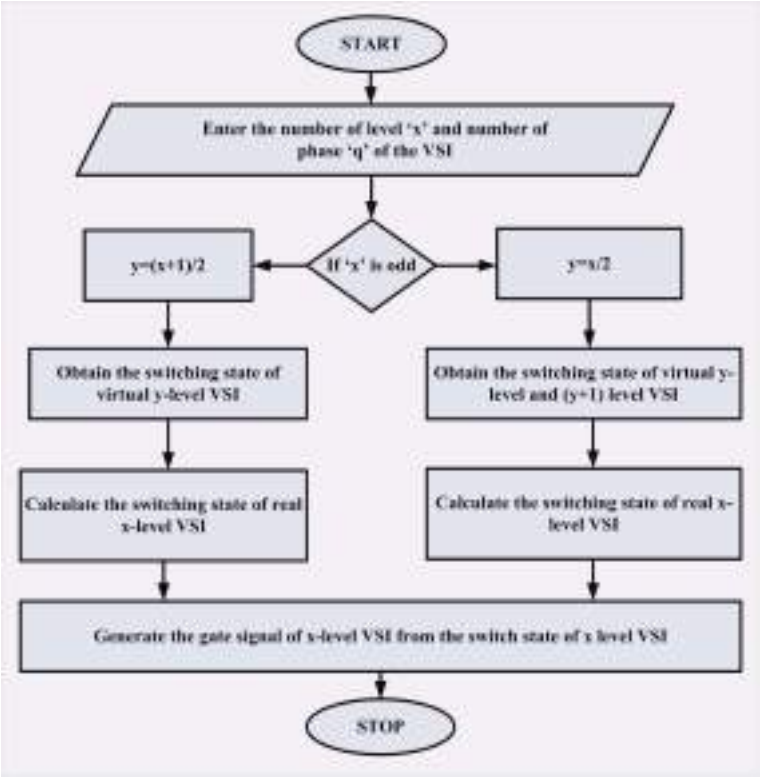
START
Enter the number of level 'x' and number of phase 'q' of the VSI
If 'x' is odd
y=(x+1)/2
y=x/2
Obtain the switching state of virtual y-level VSI
Obtain the switching state of virtual y-level and (y+1) level VSI
Calculate the switching state of real x-level VSI
Calculate the switching state of real x-level VSI
Generate the gate signal of x-level VSI from the switch state of x level VSI
STOP

Figure 6.8. Algorithm Depicted in Flowchart

of virtual y-level VSI generates maximum output from a given DC bus voltage. This is achieved by setting the value of 'j' as follows:
for even number of phases q

$$j = \frac{q}{2} \tag{6.5.5}$$

for an odd number of phases q

$$j = \frac{(q-1)}{2} \tag{6.5.6}$$

Modulation index M can be defined as

$$M = \frac{V_1}{0.5 \cdot V_{dc}} \tag{6.5.7}$$

where V_1 is the peak value of maximum pole voltage. For linear modulation range $(M < 1)$ peak value of pole voltage is $\frac{V_{dc}}{2}$. Line voltage can be described as the voltage difference between two poles of the VSI and it is given as:

$$V_{L-L} = V_{1-i} - V_{1-(i+j)} \tag{6.5.8}$$

The maximum phase difference for any q phase system is described as:

$$P_{max} = (1 - \frac{1}{q}) \cdot 180^{\circ} \tag{6.5.9}$$

For a three-phase system substituting q value as 3 in equation 6.5.9, we get P_{max} = 120°. Fundamental components of pole voltages of real x-level, q-phase VSI when x is odd can be obtained as:

$$V_i^x = V_i^y - V_{(i+j)}^x \tag{6.5.10}$$

To balance the neutral point imbalances some offset is added as follows :

$$V_i^x + V_{offset}^x = V_i^y + V_{offset}^{y1} - V_{(i+j)}^y + V_{offset}^{y2} \tag{6.5.11}$$

where $\frac{90^{\circ}}{q}$ is added as offset for V_{offset}^{y1} and $(\frac{90^{\circ}}{q} + (1 - \frac{1}{q}) \cdot 180^{\circ})$ is added as V_{offset}^{y2}. So for a three-phase system offsets added to the reference waves to make the instantaneous CMV zero are:

$$V_{offset}^{y1} = 30^{\circ} \tag{6.5.12}$$

$$V_{offset}^{y2} = 150^{\circ} \tag{6.5.13}$$

6.6 Simulations and Results

6.6.1 Double Modulating Non-Reversed Technique

The duty cycles for positive, negative and zero waveforms are shown in figure 6.9. The positive and negative modulating waveforms derived by adding some offsets to the original reference waves are shown in figure 6.10. The pulses generated for positive and negative modulating wave comparison are shown in figure 6.11. The switching pulses to all four switches of leg 'a' are generated in figure 6.12 using the switching logic of three-level NPC. The Common mode voltage in the non-reversed technique is shown in figure 6.14, which is quite greater than the reversed technique. The torque profile observed in this method is smoother as shown in figure 6.15. The main advantage of this method is the minimization of the problem of NPC unbalanced voltages as shown in figure 6.15.

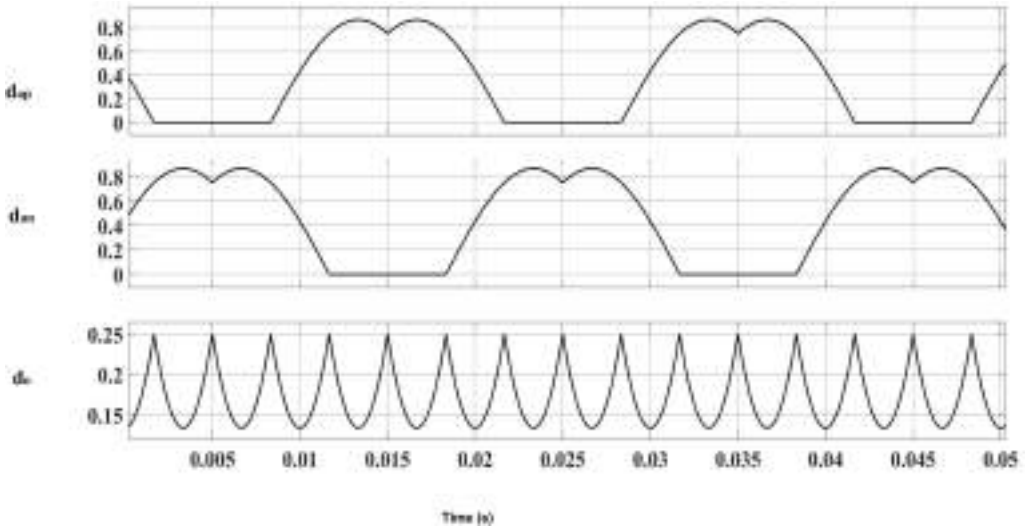

Figure 6.9. Wave Forms of Positive, Negative and Zero Duty Cycles

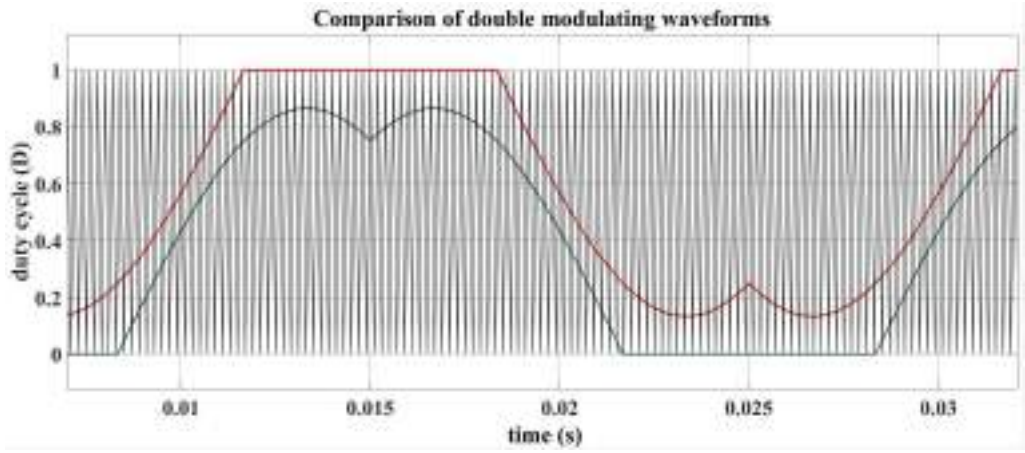

Figure 6.10. Comparison of Double Modulating Wave

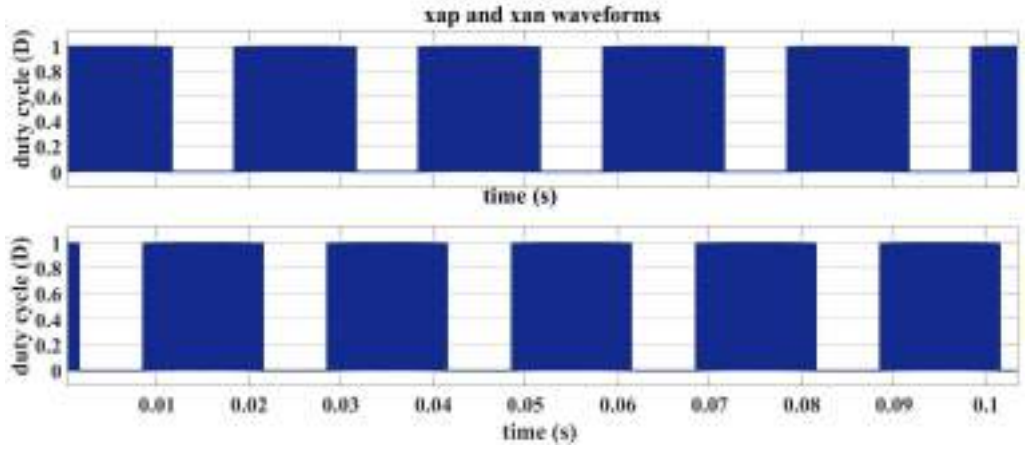

Figure 6.11. Positive and Negative Modulating Waves Pulse Generation

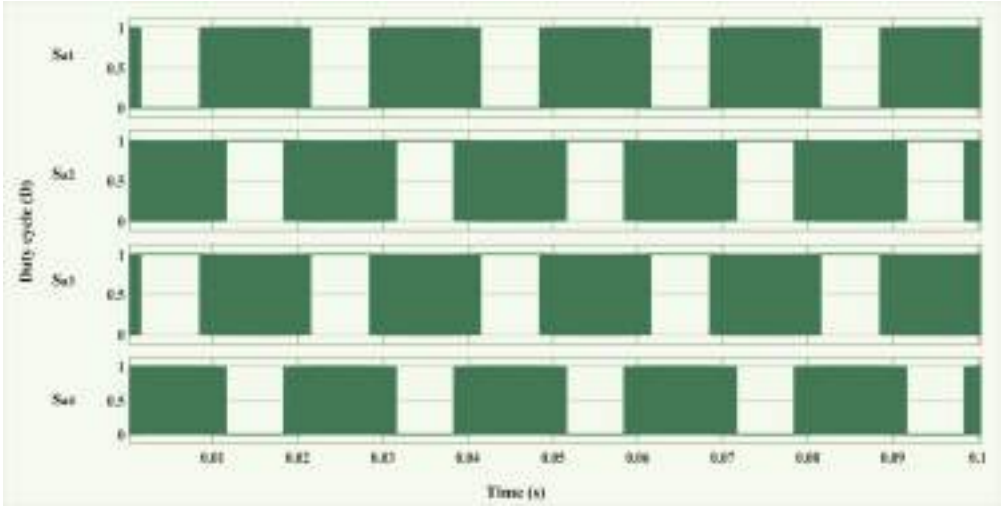

Figure 6.12. Switches Pulse Generation for Leg 'A'

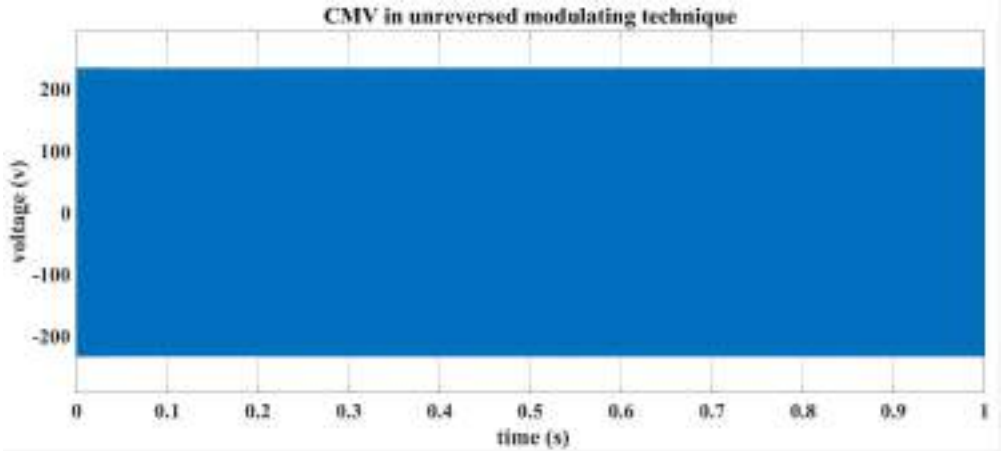

Figure 6.13. CMV in Non-Reversed Double Modulating Method

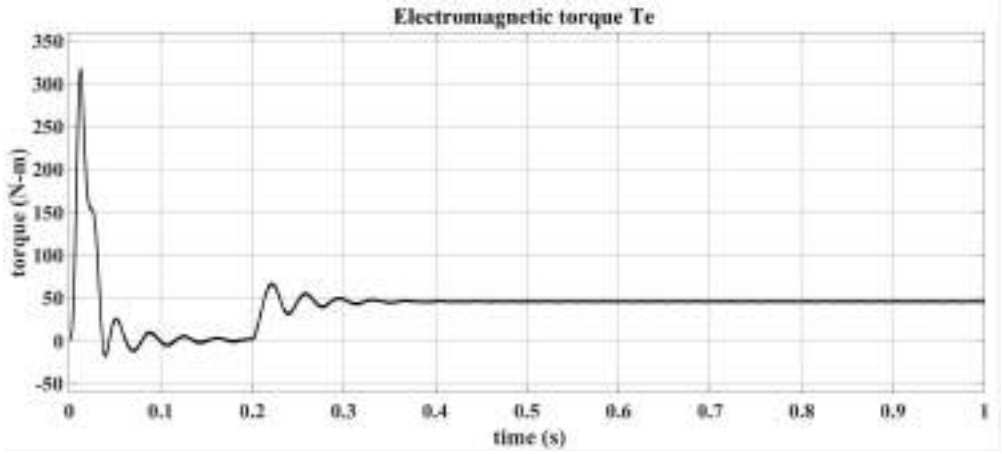

Figure 6.14. Electromagnetic Torque in Non-Reversed Double Modulating Method

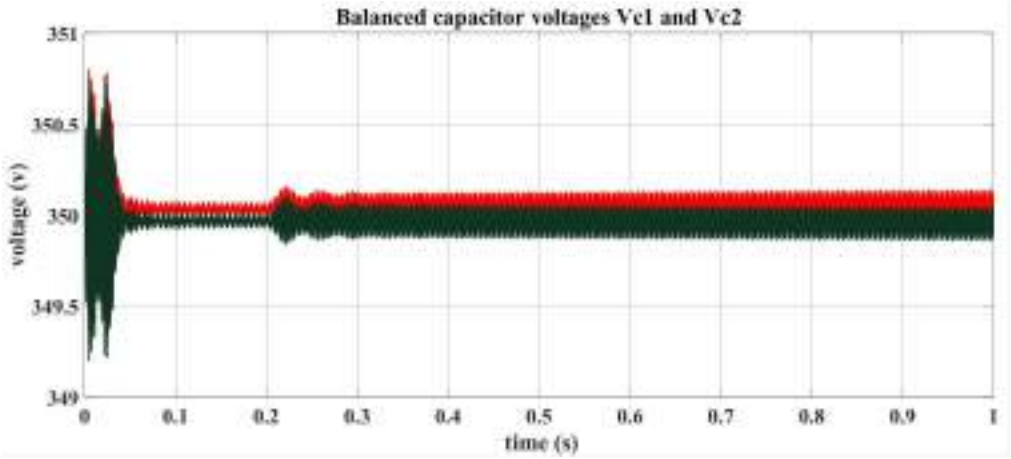

Figure 6.15. Capacitor Voltage Balancing

6.6.2 Reversed Modulating Wave Technique

The double-modulating waves U_{ap} and U_{an} are now revered and compared to generate the switching pulses. This procedure is being followed to reduce the common mode voltage along with the capacitor balancing as the CMV values are higher in the non-reversed technique. It is observed that the CMV magnitudes are drastically reduced as shown in figure 6.16. However, the torque performance is little disturbed as shown in figure 6.17.

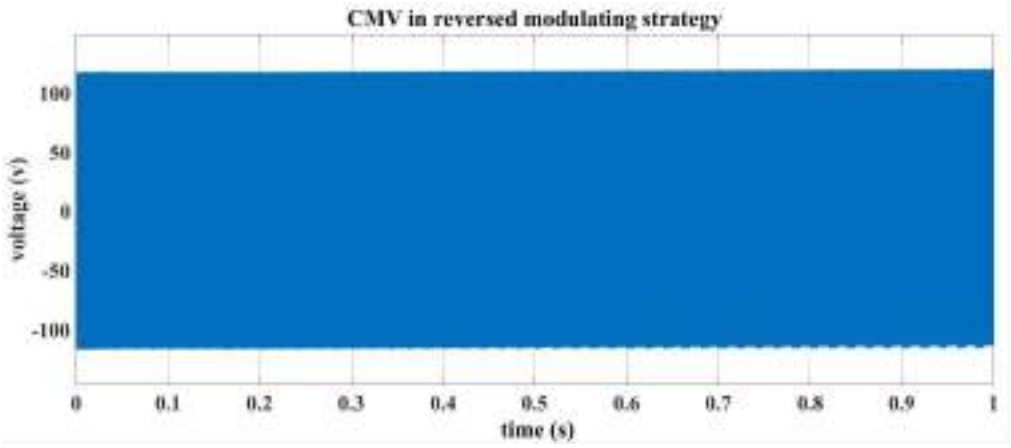

Figure 6.16. CMV in Reversed Double Modulating Method

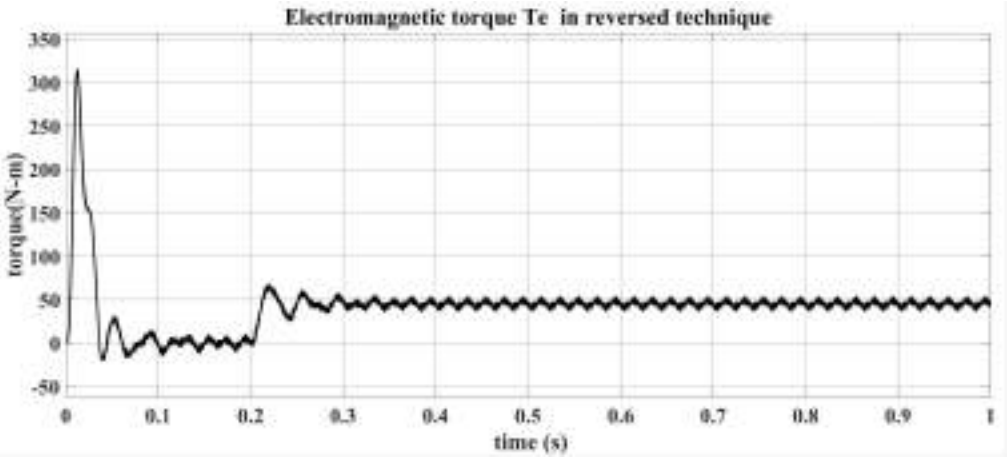

Figure 6.17. Electromagnetic Torque generated in Reversed Double Modulating Method

6.7 Carrier-Based PWM to Reduce Instantaneous CMV

In this method, the modulating waves that give maximum phase shift are considered for the comparison as shown in figure 6.18. Three level pulses by subtracting two level pulses of two legs are shown in figure 6.19. The CMV observed in this technique is almost near zero at all the instants as shown in figure 6.20, producing an RMS value of 0.267V. The torque response is also better compared to all other techniques as shown in 6.21.

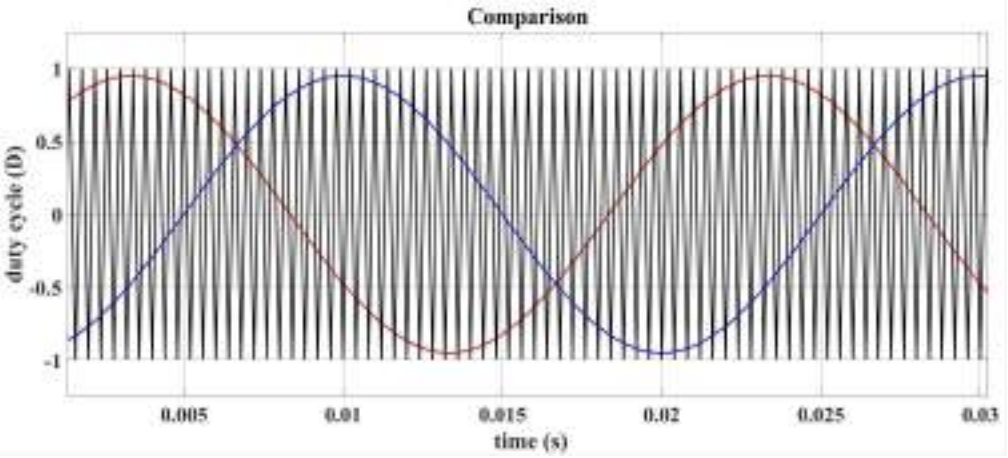

Figure 6.18. Comparison in CB-PWM Technique

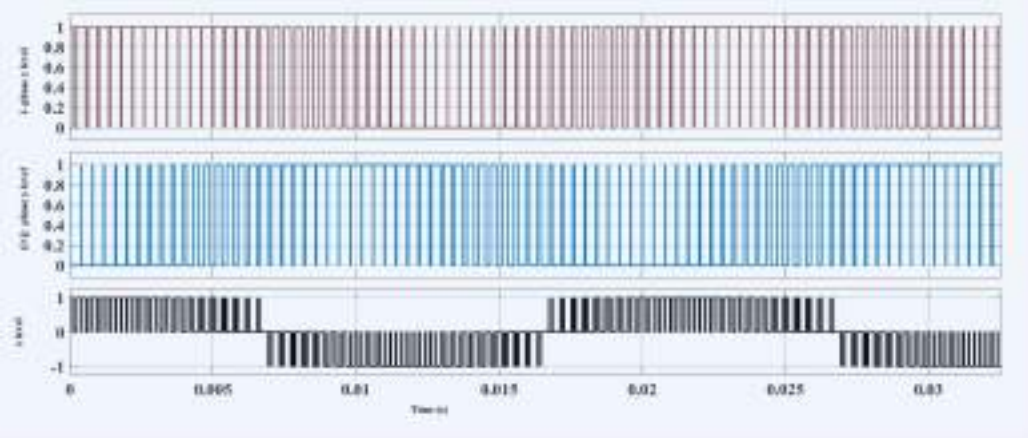

Figure 6.19. Three-level pulse generation in CB-PWM Technique

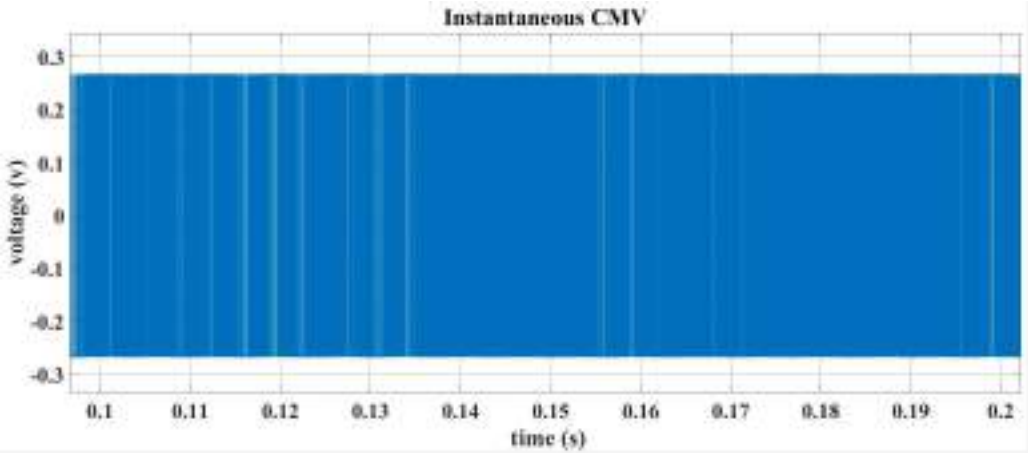

Figure 6.20. Instantaneous CMV Profile in CB-PWM Technique

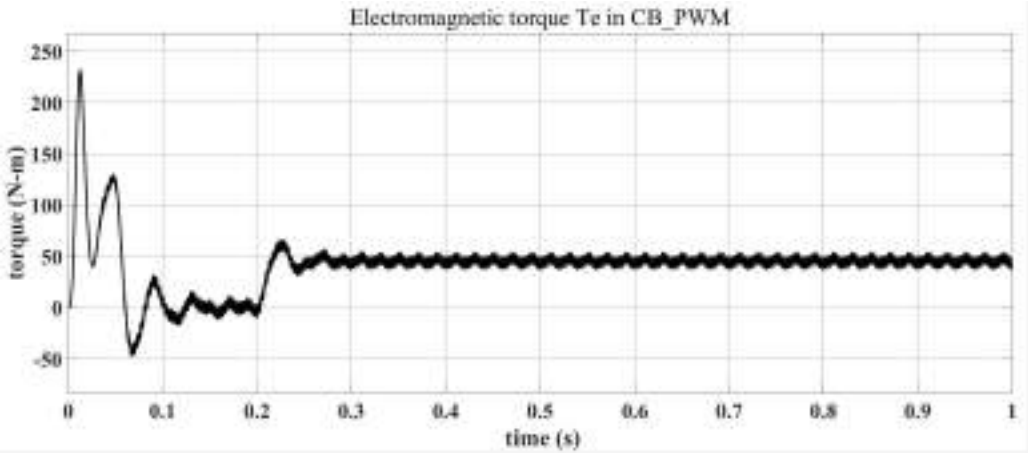

Figure 6.21. Electromagnetic Torque in CB-PWM Technique

6.8 Conclusion

The carrier-based SPWM techniques to reduce CMV have been simulated on a three-phase three-level NPC-fed induction motor as load. The prior motto of the methods performed is

to reduce the common mode voltage which induces bearing currents. These currents tend to damage the mechanical parts as well as electronic components which are near the machine. So it is quite important to reduce the shaft voltage which gets induced. Multi-level inverters provide more flexibility to reduce the high CMV-producing states compared to conventional two-level inverters. It also provides less step size of CMV voltage, which is quite helpful in reducing the magnitude of the CMV.

Double modulating wave technique is applied to reduce the neutral point oscillations and balance the capacitor voltages. The double-modulating wave technique consists of two modulating waves instead of using one modulating wave in each phase. These two modulating waves can be generated by adding some offset to the sinusoidal reference waveform as shown in the table. The main target is to resolve the problem of capacitor balancing which is quite observed in diode clamped inverters. The common mode voltage levels which are produced in non-reversal double-modulating wave techniques are $\frac{V_{dc}}{6}$, -$\frac{V_{dc}}{6}$, $\frac{V_{dc}}{3}$, -$\frac{V_{dc}}{3}$ and 0.

However, to further reduce the CMV and maintain the capacitor balancing, the modulating waveforms are reversed and compared with the same carrier. The CMV then observed is of only 3 levels which are of $\frac{V_{dc}}{6}$, -$\frac{V_{dc}}{6}$ and 0. Also, the capacitor voltages of NPC are balanced.

The electromagnetic torque observed in the reversal method contains little more ripple as compared to a non-reversal method as shown in the figure. The THD values also increase to a small extent.

The above technique holds a constraint to further reduce the CMV level. As a result, another Carrier-based PWM to reduce the instantaneous CMV value to nearly zero is simulated and analyzed. This method is quite applicable to any multi-phase and multi-level drive system. It works on the principle of transformation of the real level virtual level of the VSI and then generates the pulses. In this chapter, this technique is applied to a three-phase(q=3) and three-level (x=3) system. In, this technique for the comparison two modulating waveforms and one carrier are used. The modulating waveforms are displaced by some phase difference (P_{max} = 120°) and an offset is added to each of them as V_{offset}^{y1} and V_{offset}^{y2}. A three-level is generated by subtracting the pulses of these two levels and giving them to the VSI. The instantaneous common mode voltage has an rms value of 0.267, which is almost nearly zero. The THD is also reduced in this CB-PWM method compared to the double modulating technique.

Chapter 7

MULTI-PHASE DRIVES and it's CMV REDUCING TECHNIQUES

7.1 Comparison of $3-\varphi$ and $5-\varphi$ Induction Motors

Whereas a fault in any two phases leads to inoperative conditions in a $3-\varphi$ induction motor system, the $5-\varphi$ system produces approximately 85% of the rated power output. Hence the $5-\varphi$ system has high fault tolerant capability [24–26] compared to the $3-\varphi$ system.The current per phase reduces with the increase in the number of phases and without increasing the voltage per phase. Minimum torque ripple is observed in the $5-\varphi$ induction motor compared to the $3-\varphi$ induction motor. The loss of one or two phases does not stop the machine from starting and running in the $5-\varphi$ induction motor. Also, the $5-\varphi$ machines have a higher fault tolerant potential. At the start of the induction motor,

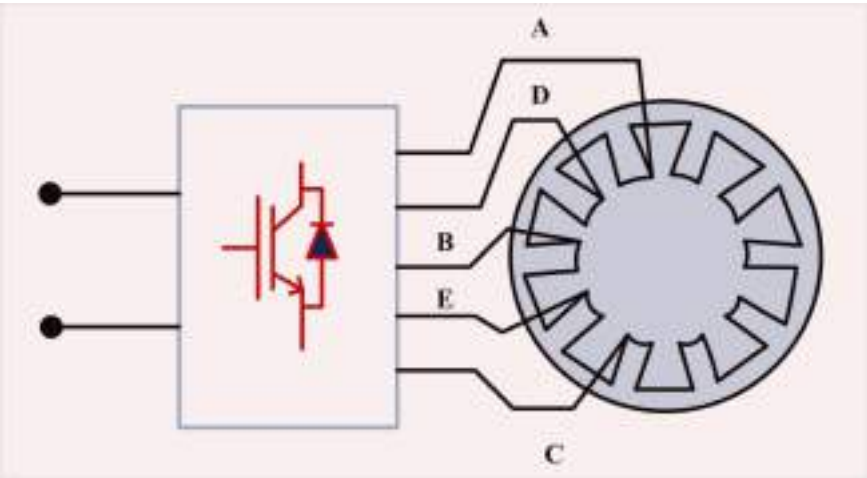

Figure 7.1. Five-Phase Drive

the inrush current flows through the motor which lasts for a few cycles and disappears as the motor attains the steady state speed. The constant no load steady-state current in stator

after high starting current. Figure 7.1 is $5-\varphi$ drive using inverter.

The mathematical model equations for d-q components and torque equation are identical to the $3-\varphi$ induction machine. The difference between the $5-\varphi$ machine model and the $3-\varphi$ machine model is the presence of voltage and flux components. The x-y components of the rotor are fully decoupled from the d-q components of each other. As the rotor is short-circuited the x-y components do not appear in the rotor circuit. Zero sequence components are omitted in both stator and rotor winding due to a short circuit in the rotor and star connection of the stator. So, finally, the x-y components are omitted in the discussion of a $5-\varphi$ induction motor in an arbitrary reference frame which makes it equal to the $3-\varphi$ induction machine and the same control schemes can be applied to a $5-\varphi$ induction motor as in $3-\varphi$ induction motor.

The x-y components correspond to certain voltage and current harmonics and this order depends on the number of phases in the stator. Hence the inverter, used to supply a multiphase induction machine, must not create low-order voltage harmonics that will excite stator current low-order harmonic flow in x-y circuits.

7.2 Five-Phase Induction Motor Modeling

In a multi-phase induction motor, the stator carries an n-phase winding while the rotor is of squirrel cage type. The stator winding is fed from a $5-\varphi$ supply. The $5-\varphi$ supply is obtained from a single-phase or $3-\varphi$ utility power supply through a diode bridge rectifier inverter circuit. The rotor winding derives its voltage and power from the externally energized stator winding through the electromagnetic induction principle. The phases are mutually displaced by $\frac{2\pi}{5}$ degrees. Equal phase displacement is achieved in the $3-\varphi$ while unequal phase displacement is observed in the $5-\varphi$ induction motor. It is very important to have a feature of an intrinsic fault-tolerant capability in the motor. Fractional slot winding motors with non-overlapped coils are suitable for fault-tolerant applications as they allow a physical separation between the phases, which ultimately limits the propagation of faults. They also have high self-inductance which limits the short-circuit current. Also, a suitable combination of slots and poles results in lowering the mutual coupling between the phases. To have a good performance the mutual coupling is preferred to be less among the phases so that when the fault occurs in one phase it doesn't get transferred to the other.

The dynamic behavior of an induction motor can be described by the parameters like voltage and torque equations. Converting the change of variables to time-varying from time-invariant helps in reducing the complexity of the motor. By using this a multiphase winding can be reduced to two-phase winding i.e. d-q axes which are quadrature to each other. The

stator and rotor variables can be transferred to an arbitrary reference frame. The steady-state model and equivalent circuit diagram help in studying the machine's performance in a steady state. The dynamic model of the induction motor is derived by using a two-phase motor in direct and quadrature d-q axes. This approach is desirable because of the conceptual simplicity obtained with two sets of windings, one on the stator and the other on the rotor. An induction motor can be represented by a mathematical model. The $5-\varphi$ system variables are transformed into $2-\varphi$ variables on a d-q plane rotating with a synchronous speed. The displacement between the two phases is 72° with the same number of phases before and after the transformation. Figure 7.2 is Mathematical Modeling Diagram of Five-Phase Induction Motor [22].

The machine model in its original form is transformed using decoupling (Clarke's) transformation matrix as follows:

$$\begin{bmatrix} V_d \\ V_q \\ V_x \\ V_y \\ V_0 \end{bmatrix} = \frac{2}{5} \begin{bmatrix} \sin\theta & \sin\left(\theta-\frac{2\pi}{5}\right) & \sin\left(\theta-\frac{4\pi}{5}\right) & \sin\left(\theta+\frac{4\pi}{5}\right) & \sin\left(\theta+\frac{2\pi}{5}\right) \\ \cos\theta & \cos\left(\theta-\frac{2\pi}{5}\right) & \cos\left(\theta-\frac{4\pi}{5}\right) & \cos\left(\theta+\frac{4\pi}{5}\right) & \cos\left(\theta+\frac{2\pi}{5}\right) \\ \sin\theta & \sin\left(\theta+\frac{4\pi}{5}\right) & \sin\left(\theta-\frac{2\pi}{5}\right) & \sin\left(\theta+\frac{2\pi}{5}\right) & \sin\left(\theta-\frac{4\pi}{5}\right) \\ \cos\theta & \cos\left(\theta+\frac{4\pi}{5}\right) & \cos\left(\theta-\frac{2\pi}{5}\right) & \cos\left(\theta+\frac{2\pi}{5}\right) & \cos\left(\theta-\frac{4\pi}{5}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ V_e \end{bmatrix}$$

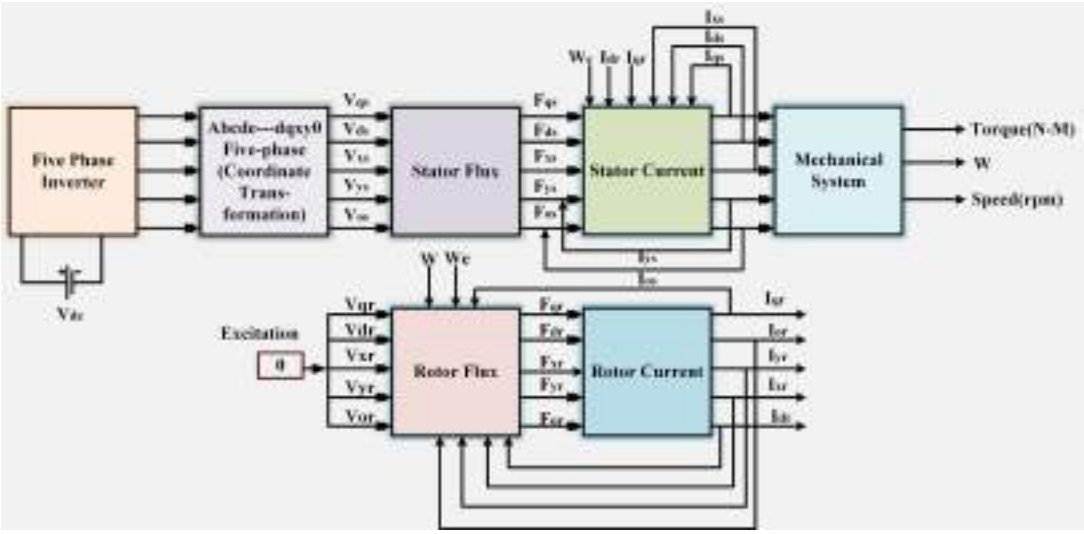

Figure 7.2. Mathematical Modeling Diagram of Five-Phase Induction Motor.

7.2.1 Stator Voltage Equations

Five-phase stator voltage of the induction motor under balanced conditions is expressed as follows:

$$V_a = \sqrt{2} \cdot V_{rms} \cdot \sin(\omega t) \tag{7.2.1}$$

$$V_b = \sqrt{2} \cdot V_{rms} \cdot \sin(\omega t - \frac{2 \cdot \pi}{5}) \tag{7.2.2}$$

$$V_c = \sqrt{2} \cdot V_{rms} \cdot \sin(\omega t - \frac{4 \cdot \pi}{5}) \tag{7.2.3}$$

$$V_d = \sqrt{2} \cdot V_{rms} \cdot \sin(\omega t + \frac{4 \cdot \pi}{5}) \tag{7.2.4}$$

$$V_e = \sqrt{2} \cdot V_{rms} \cdot \sin(\omega t + \frac{2 \cdot \pi}{5}) \tag{7.2.5}$$

Where V_a, V_b, V_c, V_d and V_e are phase voltages of $5 - \varphi$ system.As stator-to-rotor coupling takes place in only d-q equations, rotational transformation is applied to these two pairs of equations. The nature of this equation is identical to the $3 - \varphi$ machine equations. Assuming that the machine equations are transformed into an arbitrary frame of references rotating at angular speed, ω_a, the model of a $5 - \varphi$ induction machine with Stator side voltage equations in the d and q reference frame is given as follows:

$$V_{ds} = R_s \cdot I_{ds} + \frac{d\lambda_{ds}}{dt} - \omega_a \cdot \lambda_{qs} \tag{7.2.6}$$

$$V_{qs} = R_s \cdot I_{qs} + \frac{d\lambda_{qs}}{dt} - \omega_a \cdot \lambda_{ds} \tag{7.2.7}$$

$$V_{xs} = R_s \cdot I_{xs} + \frac{d\lambda_{xs}}{dt} \tag{7.2.8}$$

$$V_{ys} = R_s \cdot I_{ys} + \frac{d\lambda_{ys}}{dt} \tag{7.2.9}$$

$$V_{os} = R_s \cdot I_{os} + \frac{d\lambda_{os}}{dt} \tag{7.2.10}$$

Figure 7.3 and 7.4 show the d-axis and q-axis stator voltage waveforms.

7.2.2 Rotor Voltage Equations

$$V_{dr} = R_r \cdot I_{dr} + \frac{d\lambda_{dr}}{dt} - (\omega_a - \omega) \cdot \lambda_{qr} \tag{7.2.11}$$

$$V_{qr} = R_r \cdot I_{qr} + \frac{d\lambda_{qr}}{dt} - (\omega_a - \omega) \cdot \lambda_{dr} \tag{7.2.12}$$

$$V_{xr} = R_r \cdot I_{xr} + \frac{d\lambda_{xr}}{dt} \tag{7.2.13}$$

$$V_{yr} = R_r \cdot I_{yr} + \frac{d\lambda_{yr}}{dt} \tag{7.2.14}$$

$$V_{or} = R_r \cdot I_{or} + \frac{d\lambda_{or}}{dt} \tag{7.2.15}$$

7.2.3 Flux Equations

Stator Side Flux Linkages

$$\lambda_{ds} = (L_s + L_m) \cdot I_{ds} + L_m \cdot I_{dr} \tag{7.2.16}$$

$$\lambda_{qs} = (L_s + L_m) \cdot I_{qs} + L_m \cdot I_{qr} \tag{7.2.17}$$

$$\lambda_{xs} = L_s \cdot I_{xs} \tag{7.2.18}$$

$$\lambda_{ys} = L_s \cdot I_{ys} \tag{7.2.19}$$

$$\lambda_{os} = L_s \cdot I_{os} \tag{7.2.20}$$

Rotor Side Flux Linkages

$$\lambda_{dsr} = (L_r + L_m) \cdot I_{dr} + L_m \cdot I_{ds} \tag{7.2.21}$$

$$\lambda_{qr} = (L_r + L_m) \cdot I_{qr} + L_m \cdot I_{qs} \tag{7.2.22}$$

$$\lambda_{xr} = L_r \cdot I_{xr} \tag{7.2.23}$$

$$\lambda_{yr} = L_r \cdot I_{yr} \tag{7.2.24}$$

$$\lambda_{or} = L_r \cdot I_{or} \tag{7.2.25}$$

Where,

$$L_m = \frac{(n)}{2} \cdot M \tag{7.2.26}$$

M is the maximum value of the stator-to-rotor mutual inductances in the phase-variable model. Symbols R and L stand for resistance and inductance, v, i, and c denote voltage, current, and flux linkage, while indices s, and r identify stator/rotor variables/parameters. Index l identifies leakage inductances.

From the above equations, the torque and speed can be obtained as follows:

$$T_e = \frac{5}{2} \cdot \frac{P}{2} \cdot \frac{1}{\omega_b} \cdot (\lambda_{ds} i_{qs} - \lambda_{ds} i_{qs}) \tag{7.2.27}$$

$$\omega_r = \frac{P}{2 \cdot J} \cdot (T_e - T_l) \tag{7.2.28}$$

Where, P is the number of poles; J moment of inertia; T_l is Load Torque; T_e is Electromechanical torque ; ω_r is Rotor Speed. Once the stator voltage V_a,V_b,V_c,V_d, and V_e are transformed to d-q frame then we implement the flux linkages equations, current equations, torque equations, and rotor speed equations to obtain current in terms of I_{qs},I_{ds},I_{qr} and I_{dr} then we use inverse transformation equations to obtain the stator currents in machine variable form.The q-axis and d-axis stator current waveforms are depicted in Figure 7.4 and 7.5, while Figure 7.6 and 7.7 depict the d-axis and q-axis rotor current waveforms. Figure 7.9 and 7.10 show the Five-phase stator current and speed response of the motor.

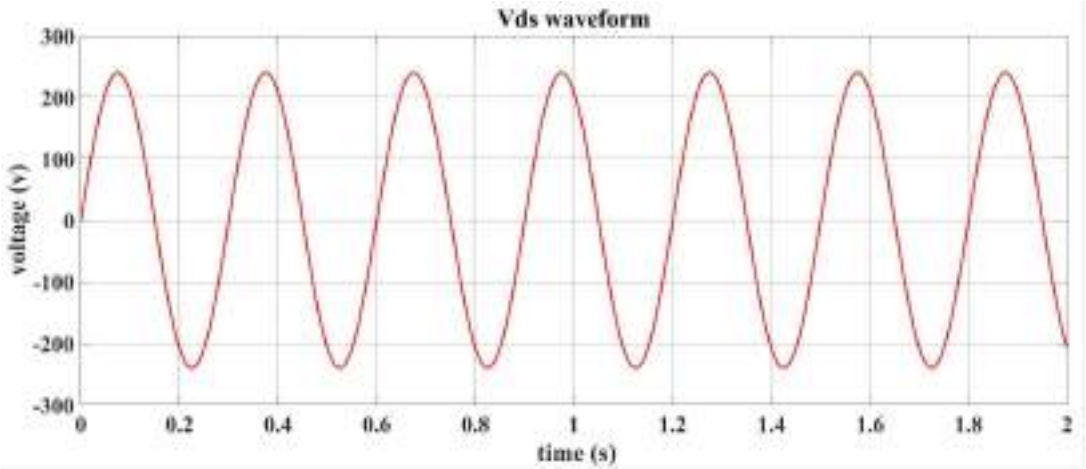

Figure 7.3. V_{ds} waveform

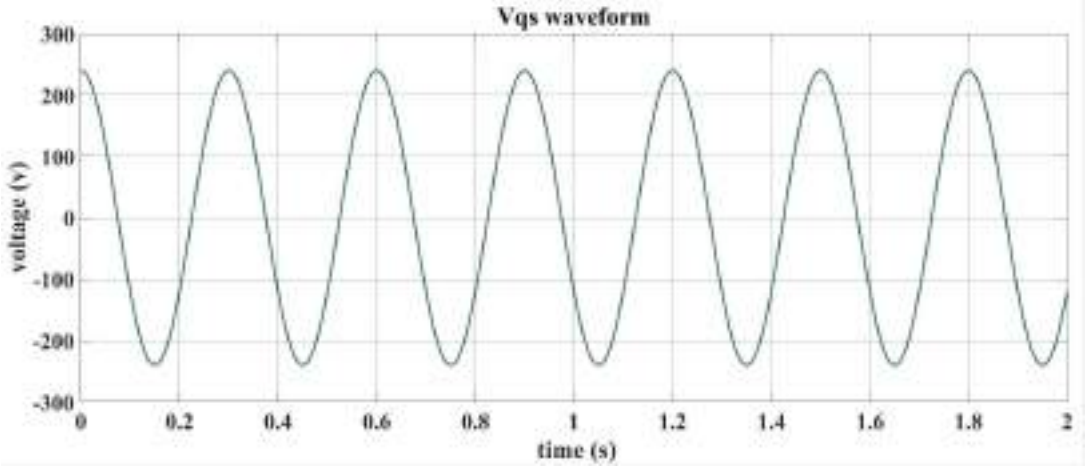

Figure 7.4. V_{qs} waveform

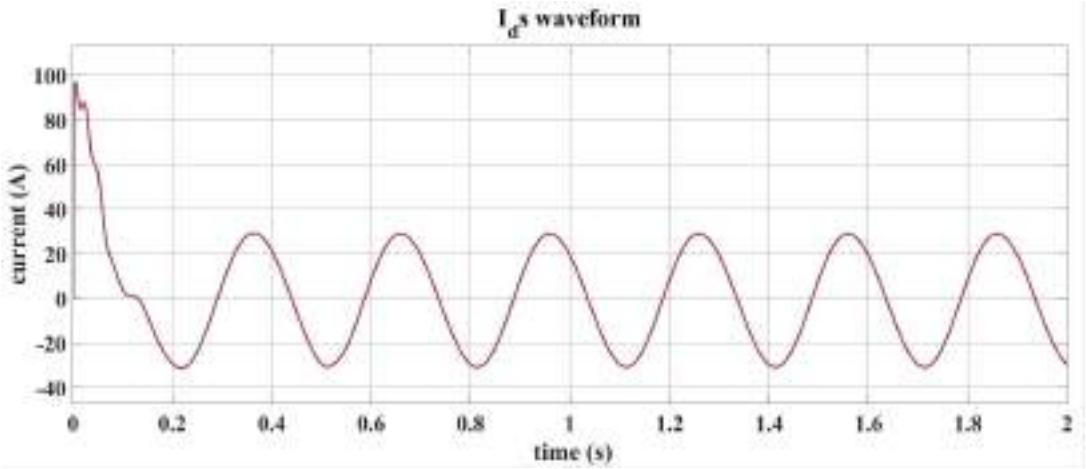

Figure 7.5. I_{ds} waveform

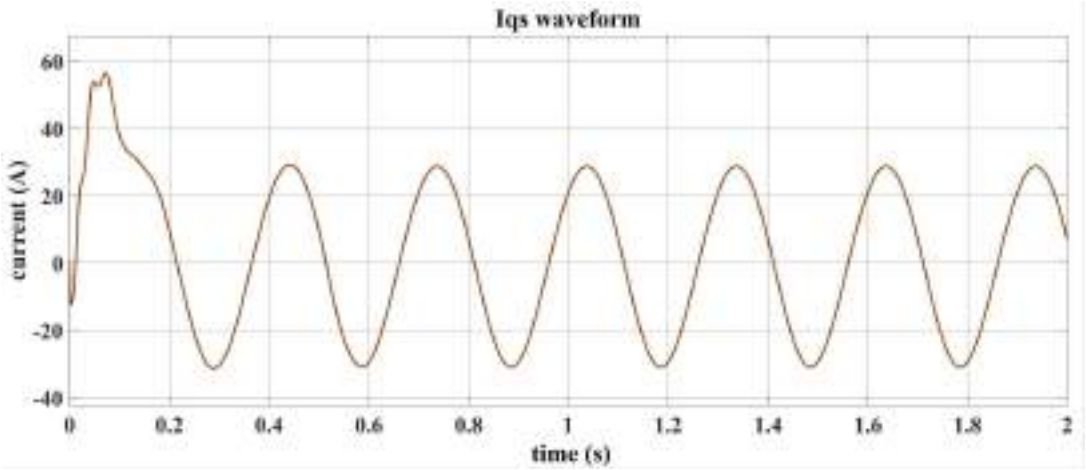

Figure 7.6. I_{qs} waveform

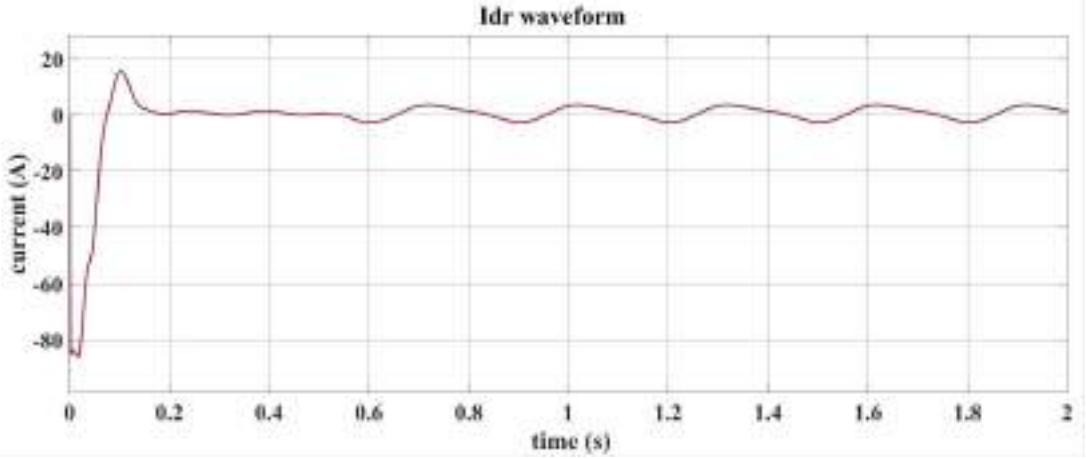

Figure 7.7. I_{dr} waveform

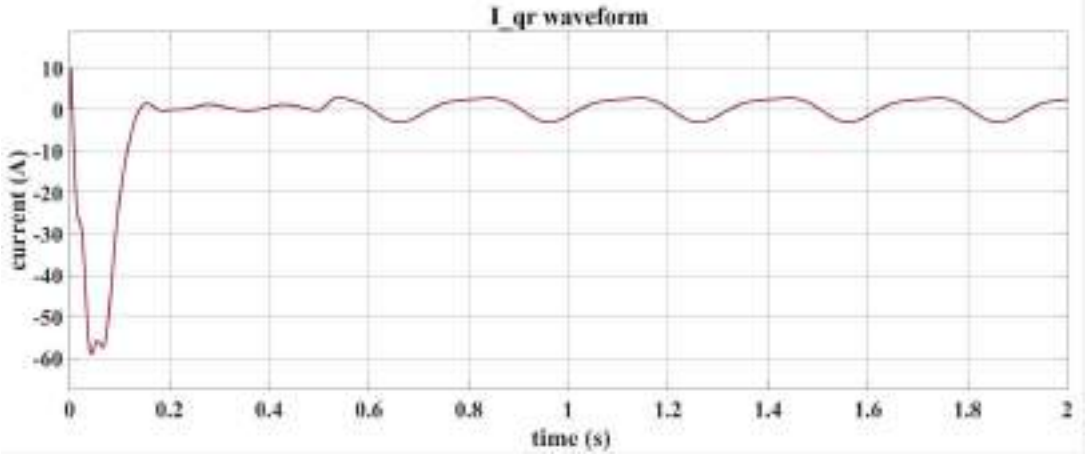

Figure 7.8. I_{qr} wave form

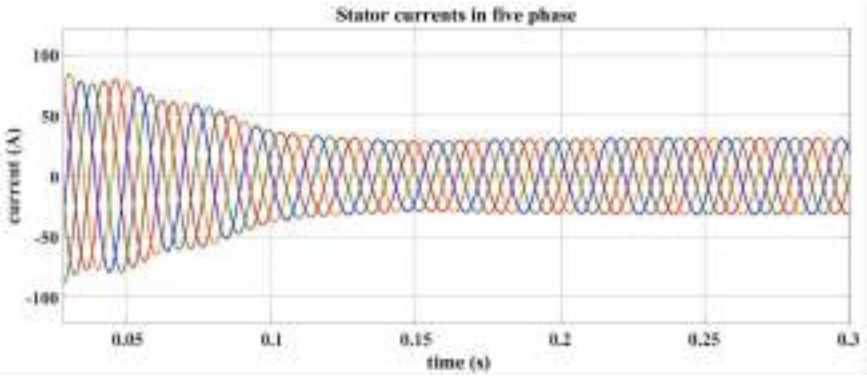

Figure 7.9. Five-Phase Stator Currents

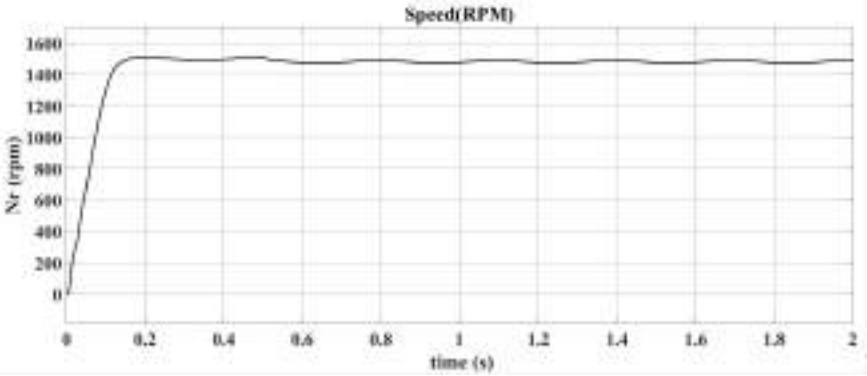

Figure 7.10. Speed Response of Five-Phase Induction Motor

7.3 SPWM Carrier Based Strategies to Reduce CMV

7.4 Carrier Displacement Techniques

When using an SPWM algorithm for a three-level VSI, it's crucial to define two key quantities. The amplitude modulation index is the ratio between the peak-to-peak amplitude of the modulating signal and the carrier waveforms. The peak-to-peak amplitude of the carrier waves is typically normalized to the DC bus voltage. One or more carrier waves may fill consecutive vertical bands. PD-SPWM and POD-SPWM algorithms [23] have two carrier bands, resulting in amplitude modulation represented as:

$$M_a = \frac{A_m}{2 \cdot A_c} \tag{7.4.1}$$

The frequency modulation index measures the impact of carrier frequency (m) on CMV and THD in comparison to the reference frequency. The frequency modulation index can be represented as:

$$M_f = \frac{f_c}{f_m} \tag{7.4.2}$$

Impacts of Carrier Frequency and Amplitude Modulation Index

The carrier frequency is a crucial factor in carrier-based PWM schemes as it affects switching losses and THD in output. The carrier frequency (f_c) affects the rms value of the CMI since it governs the CMV pulse rates (ranging from $4f_c$ to $6f_c$) . Unfortunately, f_c does not influence the CMV's peak amplitude. To avoid affecting sensitive control devices nearby, choose (f_c) to keep CMI noise levels below their thresholds. For industrial ASD applications, carrier frequencies typically range from 600 Hz to 6 kHz. However, in utility applications, f_c should be kept lower to save switching losses and EMI. The amplitude modulation index has a significant impact on ML-VSI performance, including inverter efficiency and THD in output voltage. As the amount of a m falls, inverter losses become a larger fraction of total system losses. The PWM method has fewer output states, resulting in increased distortion in the waveform. The three-level NPC VSI utilizes all levels throughout a range of a m, however inner switches S_{x2} and S_{x3} have significantly higher duty than outside switches S_{x1} and S_{x4}. Figure 7.11 is Carrier Alignment Based Techniques.

7.4.1 Phase Disposition PWM (PD-PWM)

Three-level PD-SPWM uses two triangular carriers, each with a peak-to-peak magnitude of Ac. A DC offset of V_{dc}/2 is added to one carrier and an offset of -V_{dc}/2 is added to another carrier. The sinusoidal reference waveform is superimposed onto two carriers such that its peak-to-peak amplitude m_A is also normalized to DC bus voltage. The same carriers will be used for other phases, whereas the reference waveforms change for each phase. The switching logic for a three-level single phase can be determined as

$$S_{x1} = 1, V_{refx} >= V_{cupper}; 0, otherwise \tag{7.4.3}$$

$$S_{x2} = 1, Vref_x > V_{clower}; 0, otherwise \tag{7.4.4}$$

$$S_{x3} = 1, V_{refx} < V_{cupper}; 0, otherwise \tag{7.4.5}$$

$$S_{x4} = 1, V_{refx} <= V_{clower}; 0, otherwise \tag{7.4.6}$$

Where V_{ref_x} is the reference waveform V_{c_upper} is the upper carrier wave and V_{c_lower} is the lower carrier waveform.

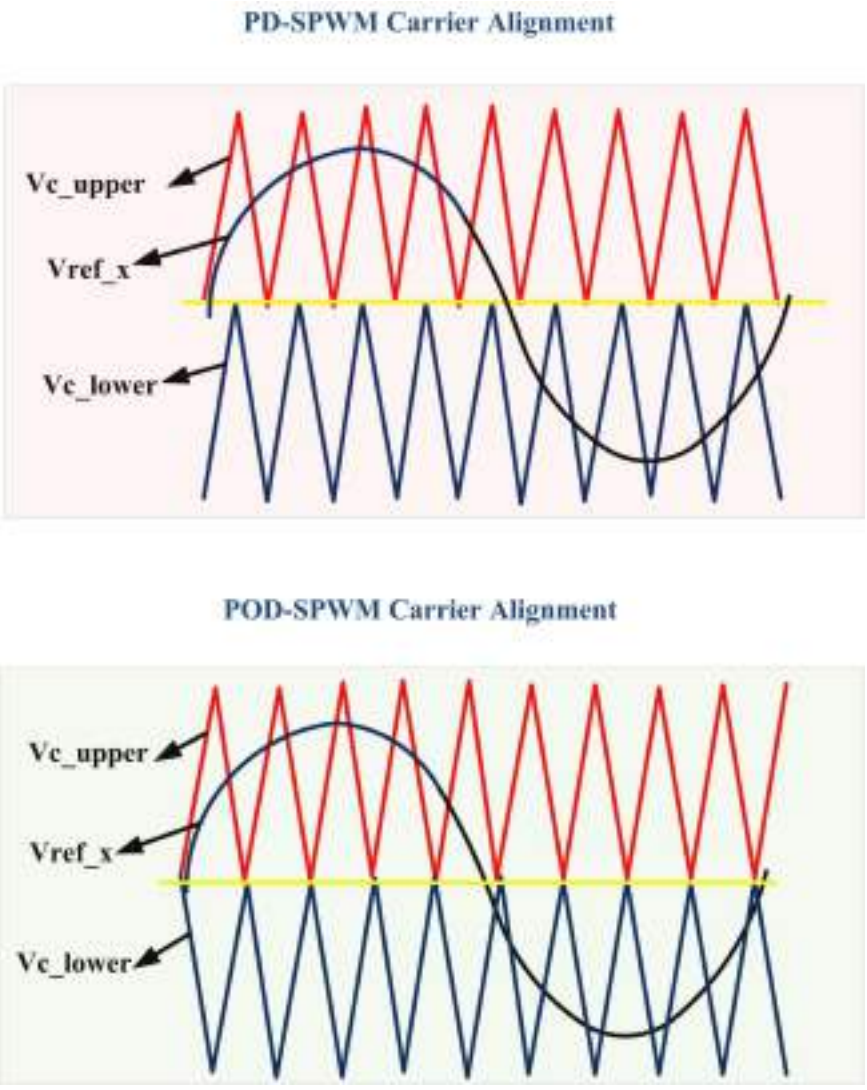

Figure 7.11. Carrier Alignment Based Techniques

7.4.2 Phase-Opposite-Disposition PWM (POD-SPWM)

This technique applies the definition of CMV and the line-to-line three-phase voltage principle to generate only seven states that produce zero CMV. Two carrier waves are displaced by a phase shift of 180 degrees as shown in the Figure 7.11 is Carrier Alignment Based Techniques.

7.4.3 Simulations and Results

Phase disposition (PD) and phase opposite disposition (POD) are simplest the carrier displacement PWM control techniques performed to control the drive performance. In phase disposition techniques the carriers are placed in phase with each other. As the converter is

of a five-phase, three-level configuration, the number of carriers required is 2. The torque in PD-SPWM is smoother when compared to the torque in the POD technique. The CMV which is observed using the POD technique is quite lesser compared to all other SPWM and SVPWM techniques. Moreover, the torque performed is not degraded using the POD technique. As it requires only two carriers both POD and Alternate phase opposition disposition APOD techniques are the same in this configuration. Figure 7.12 and 7.14 show the plots for Phase-Disposition PD-SPWM Technique and Phase-Opposite-Disposition POD-SPWM Technique, respectively.

The CMV levels produced in PD-SPWM are $\pm\frac{V_{dc}}{10}$, $\pm\frac{V_{dc}}{5}$, $\pm\frac{V_{dc}}{3}$. Whereas the CMV levels produced by POD-SPWM are $\pm\frac{V_{dc}}{10}$ and 0. The magnitude of CMV is decreased drastically as the multi-phase and multi-level configurations are adopted. The step change in CMV is much less compared to conventional two-level configurations. Further, the CB-PWM technique observed in a three-phase, three-level converter to minimize the instantaneous CMV to zero can also be extended to a five-phase three-level.Figure 7.13 and 7.15 show the common mode voltage (CMV) plots for PD-SPWM and POD-SPWM, respectively.

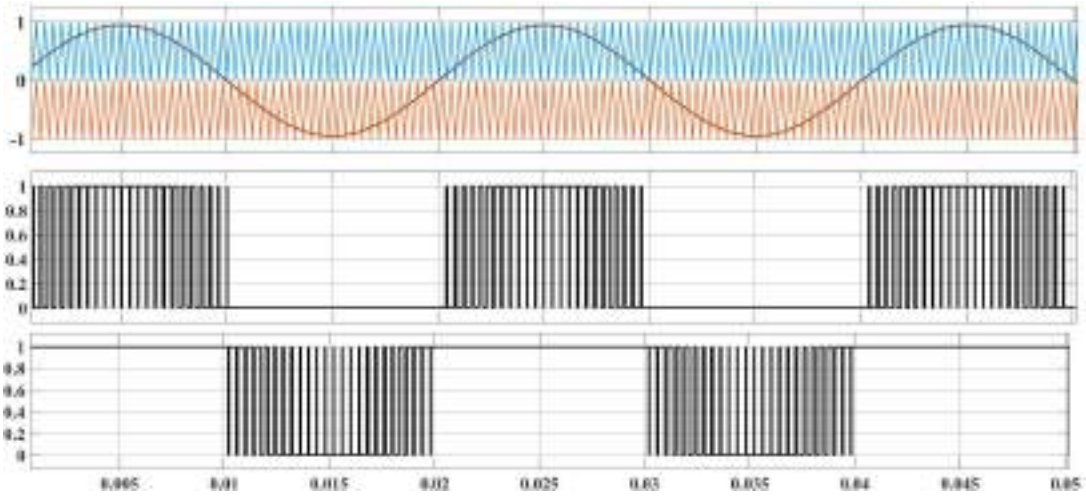

Figure 7.12. Phase-Disposition PD-SPWM Technique

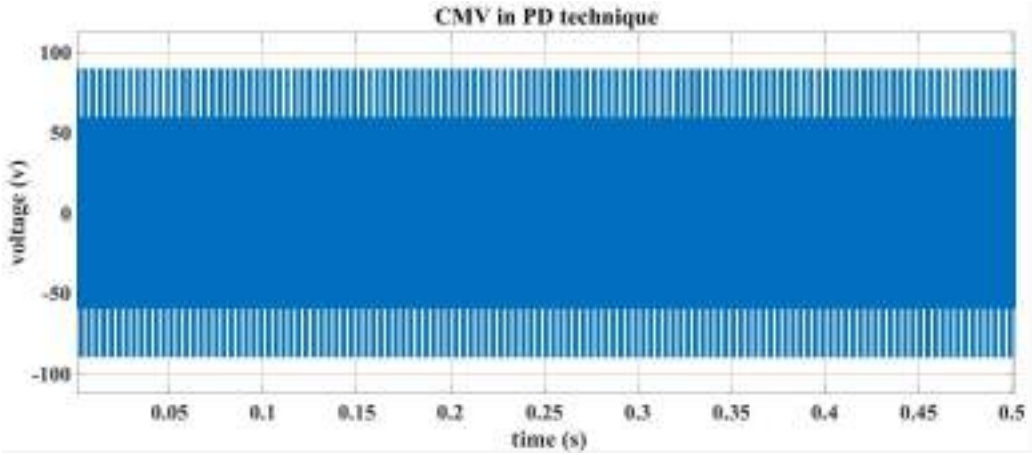

Figure 7.13. CMV in PD-SPWM

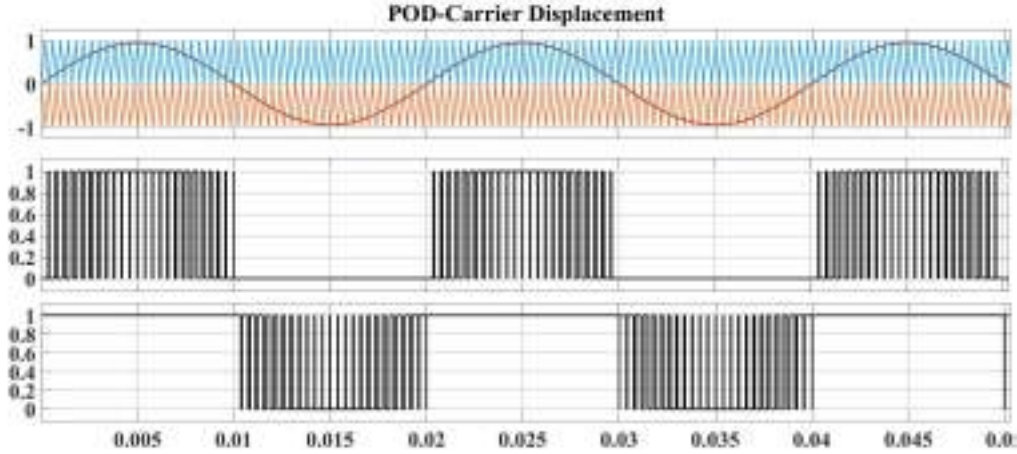

Figure 7.14. Phase-Opposite-Disposition POD-SPWM Technique

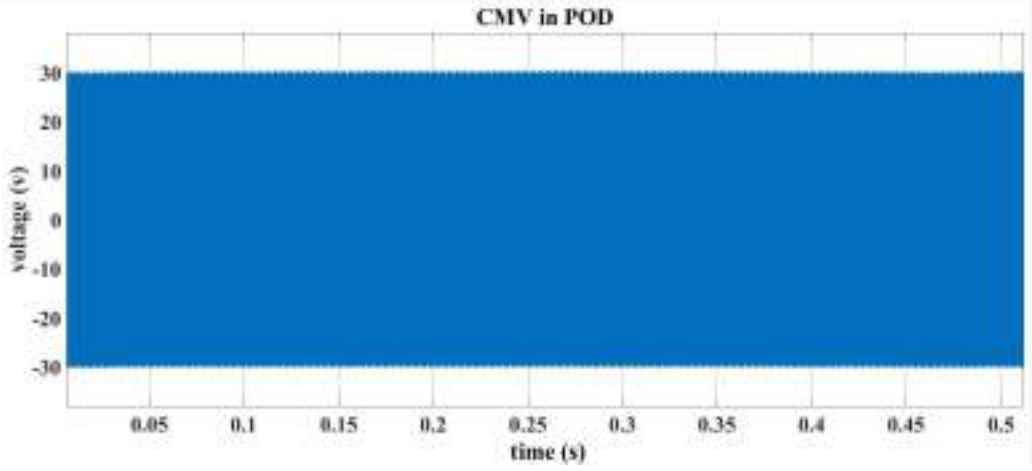

Figure 7.15. CMV in POD-SPWM

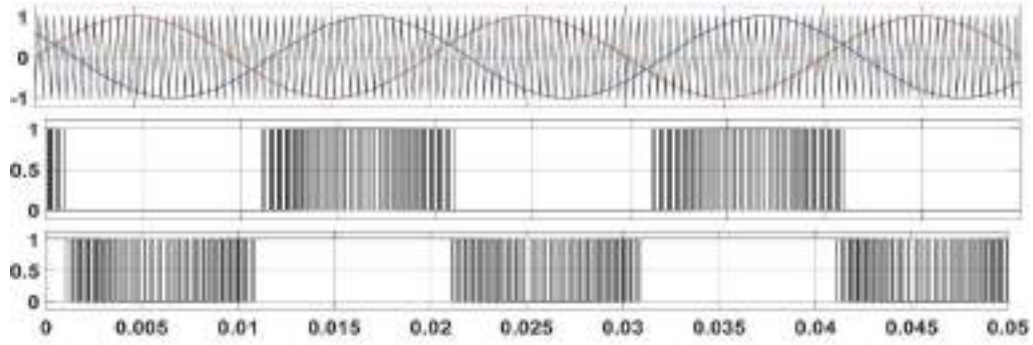

Figure 7.16 Proposed SPWM Technique

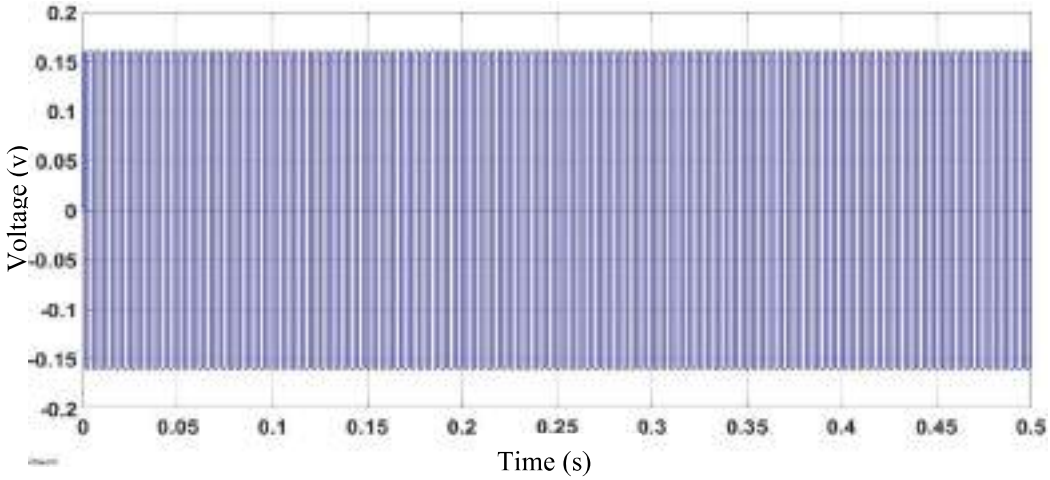

Figure 7.17. CMV in Proposed-SPWM

7.5 Conclusion

A five-phase induction motor is modelled and connected to the three-level NPC. The working of NPC is the same as discussed in Chapter 6. The control logic applied here are the PD and POD techniques which are easy to control and Proposed SPWM Technique produce lesser common mode voltages with better torque and speed characteristics.

Future Scope

This thesis presented various common mode voltage mitigation techniques on different drive systems. Out of all the techniques, the CMV reduced by carrier based PWM which can reduce the instantaneous CMV to almost zero was more advantageous. It also produced a good electromagnetic torque profile. The hardware required by this method is comparatively less. In this thesis, mitigation is performed on a three-phase, three-level NPC configuration. This technique can easily extended to multi-phase and multi-level systems which can be further more advantageous due to redundancies.

Bibliography

[1] Tawfiq, Kotb B., Mehmet Güleç, and Peter Sergeant. ”Bearing Current and Shaft Voltage in Electrical Machines: A Comprehensive Research Review.” *Machines 11, no. 5 (2023)*: 550.

[2] Zheng, Jian, Mingcheng Lyu, Shengqing Li, Qiwu Luo, and Keyuan Huang. ”Common-mode reduction SVPWM for three-phase motor fed by two-level voltage source inverter.” Energies 13, no. 15 (2020): 3884.

[3] Zheng, Jian, Mingcheng Lyu, Shengqing Li, Qiwu Luo, and Keyuan Huang. ”Common-mode reduction SVPWM for three-phase motor fed by two-level voltage source inverter.” *Energies 13*, no. 15 (2020): 3884.

[4] Belbali, Abdelkarim, Salim Makhloufi, Abdellah Kadri, Laidi Abdallah, and Zemitte Seddik. ”Mathematical Modeling of a Three-Phase Induction Motor.” In Induction Motors-Recent Advances, New Perspectives and Applications. IntechOpen, 2023.

[5] Modi, Manoj Kumar, S. Venugopal, and G. Narayanan. ”Space vector-based analysis of overmodulation in triangle-comparison based PWM for voltage source inverter.” *Sadhana 38 (2013)*: 331-358.

[6] Narayanan, G., and V. T. Ranganathan. ”Bus-clamped PWM techniques for AC drives-Application considerations.” (2000).

[7] Narayanan, G., and V. T. Ranganathan. ”Analytical evaluation of harmonic distortion in PWM AC drives using the notion of stator flux ripple.” *IEEE Transactions on power electronics 20*, no. 2 (2005): 466-474.

[8] Narayanan, G., Harish K. Krishnamurthy, Di Zhao, and Rajapandian Ayyanar. ”Advanced bus-clamping PWM techniques based on space vector approach.” *IEEE Transactions on Power Electronics 21*, no. 4 (2006): 974-984.

[9] Nair, Meenu D., Jayanta Biswas, G. Vivek, and Mukti Barai. ”Performance Evaluation of Various Bus Clamped Space Vector Pulse Width Modulation Techniques.” *Journal of Power Electronics 17, no. 5 (2017)*: 1244-1255.

[10] Arora, T. G., M. M. Renge, and M. V. Aware. ”Effects of switching frequency and motor speed on common mode voltage, common mode current and shaft voltage in PWM inverter-fed induction motors.” In 2017 12th IEEE conference on industrial electronics and applications (ICIEA), pp. 583-588. IEEE, 2017.

[11] Narayanan, G., Di Zhao, Harish K. Krishnamurthy, Rajapandian Ayyanar, and V. T. Ranganathan. ”Space vector based hybrid PWM techniques for reduced current ripple.” *IEEE Transactions on Industrial Electronics 55, no. 4 (2008)*: 1614-1627.

[12] Mnati, Mohannad Jabbar, Dimitar V. Bozalakov, and Alex Van den Bossche. ”PID control of a three phase photovoltaic inverter tied to a grid based on a 120-degree bus clamp PWM.” *Ifac-Papersonline 51*, no. 4 (2018): 388-393.

[13] Wu, Deliang, Hafsa Qamar, Haleema Qamar, and Rajapandian Ayyanar. ”Comprehensive Analysis and Experimental Validation of 240°-Clamped Space Vector PWM Technique Eliminating Zero States for EV Traction Inverters With Dynamic DC Link.” *IEEE Transactions on Power Electronics 35*, no. 12 (2020): 13295-13307.

[14] Namilikonda, Aakanksha, B. S. Umre, L. Charan, and G. Shiva rama Krishna. ”Comparative Analysis of CMV Variation Using Different BUS Clamping SVPWM Techniques.” In 2024 Third *International Conference on Power, Control and Computing Technologies (ICPC2T)*, pp. 541-546. IEEE, 2024.

[15] Robles Pérez, Endika, Markel Fernández Zubizarreta, Jordi Zaragoza, Iker Aretxabaleta Astoreka, Iñigo Martínez de Alegría Mancisidor, and Jon Andreu Larrañaga. ”Common-Mode Voltage Elimination in Multilevel Power Inverter-Based Motor Drive Applications.” (2022).

[16] J. Rodríguez, J.-S. Lai and F. Z. Peng, ”Multilevel inverters: A survey of topologies controls and applications”, *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[17] Kadum, Arkan A. ”PWM control techniques for three phase three level inverter drives.” *TELKOMNIKA (Telecommunication Computing Electronics and Control)* 18, no. 1 (2020): 519-529.

[18] Liu, Peng, Shanxu Duan, Chuan Yao, and Changsong Chen. ”A double modulation wave CBPWM strategy providing neutral-point voltage oscillation elimination and CMV reduction for three-level NPC inverters.” *IEEE Transactions on Industrial Electronics 65, no. 1 (2017): 16-26.*

[19] Maheshwari, Ramkrishan, Stig Munk-Nielsen, and Sergio Busquets-Monge. "Design of neutral-point voltage controller of a three-level NPC inverter with small DC-link capacitors." *IEEE Transactions on Industrial Electronics* 60, no. 5 (2012): 1861-1871.

[20] J. Pou, "Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point", *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2288-2294, Aug. 2007.

[21] Chakrabarti, Abanishwar, Koustuv Sarkar, Prabir Ranjan Kasari, Bikram Das, and Sujit K. Biswas. "A CB-PWM technique for eliminating CMV in multilevel multiphase VSI." *IEEE Transactions on Industrial Electronics 70*, no. 9 (2022): 8666-8675.

[22] Saikumar, Veldandi Vamshi, B. Sathyavani, and J. Suresh. "Mathematical Modeling of Five-Phase and Three-Phase Induction Motor and their Result Comparison." In *IOP Conference Series: Materials Science and Engineering,* vol. 981, no. 4, p. 042059. IOP Publishing, 2020.

[23] Palanisamy, R., K. Vijayakumar, K. Selvakumar, D. Karthikeyan, and G. Santhoshkumar. "Implementation of 5 Phase 3 Level NPC Inverter Using Space Vector Modulation." *Indian Journal of Science and Technology* (2016).

[24] Ramasamy, Palanisamy, and Vijayakumar Krishnasamy. "Minimization of common-mode voltage for five-phase three-level NPC inverter using SVPWM strategy." *Iranian Journal of Science and Technology, Transactions of Electrical Engineering* 44 (2020): 1221-1232.

[25] Manohar, G., and S. Venkateshwarlu. "Performance Analysis of Three Level Diode Clamped Inverter fed Induction Machine using Multicarrier PWM Techniques." *CVR Journal of Science and Technology* 16, no. 1 (2019): 59-65.

[26] Jyothi, B., and M. Venu Gopala Rao. "Performance analysis of 3-level 5-phase multilevel inverter topologies." *International Journal of Electrical and Computer Engineering* 7, no. 4 (2017): 1696.